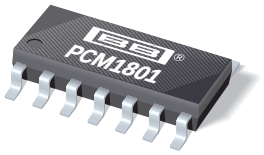
BURR - BROWN®



PCM1801

For most current data sheet and other product information, visit www.burr-brown.com

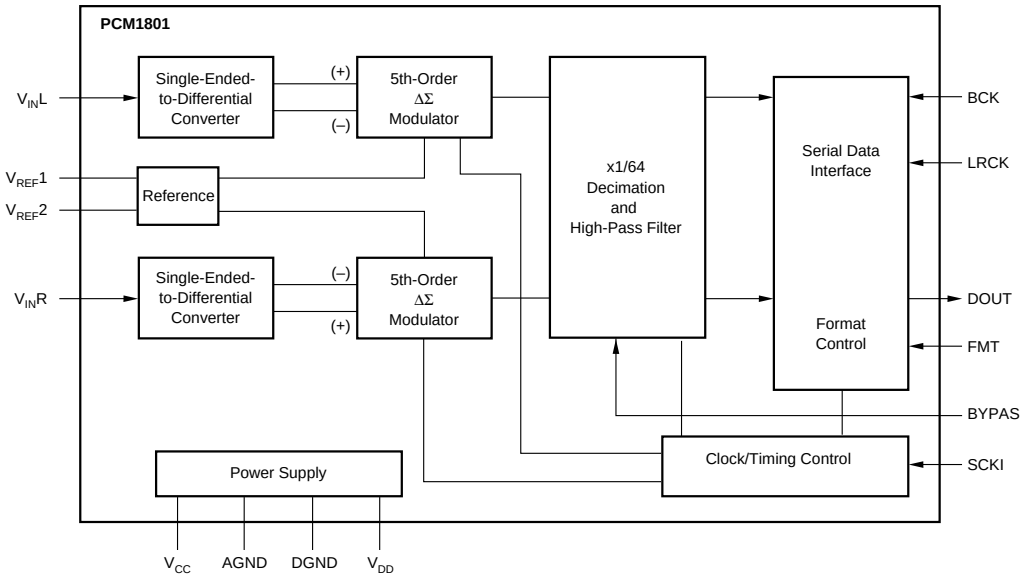
16-Bit, Stereo, Audio ANALOG-TO-DIGITAL CONVERTER

FEATURES

- DUAL 16-BIT MONOLITHIC ΔΣ ADC
- SINGLE-ENDED VOLTAGE INPUT
- 64X OVERSAMPLING DECIMATION FILTER:
  Passband Ripple: ±0.05dB
  Stopband Attenuation: –65dB
- ANALOG PERFORMANCE:
  THD+N: –88dB (typ)
  SNR: 93dB (typ)
  Dynamic Range: 93dB (typ)
  Internal High-Pass Filter
- PCM AUDIO INTERFACE: Left Justified, I²S
- SAMPLING RATE: 4kHz to 48kHz
- SYSTEM CLOCK: 256f_S, 384f_S, or 512f_S
- SINGLE +5V POWER SUPPLY
- SMALL SO-14 PACKAGE

DESCRIPTION

PCM1801 is a low cost, single chip stereo analog-to-digital converter with single-ended analog voltage inputs. The PCM1801 uses a delta-sigma modulator with 64x oversampling, a digital decimation filter, and a serial interface which supports Slave mode operation and two data formats. The PCM1801 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required.



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Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

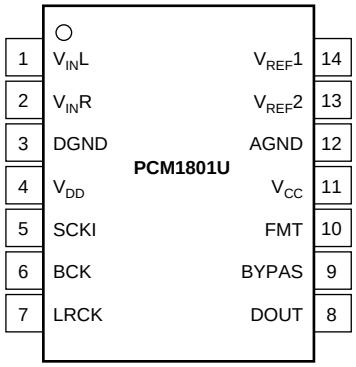
All specifications at +25°C, $+V_{DD}$ = $+V_{CC}$ = +5V, f_S = 44.1kHz, and 16-bit data, SYSCLK = 384f_S, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1801U MIN	PCM1801U TYP	PCM1801U MAX	UNITS
RESOLUTION			16		Bits
DIGITAL INPUT/OUTPUT					
Input Logic Level:					
V_{IH}(1)		2.0			V
V_{IL}(1)				0.8	V
Input Logic Current:					
I_{IN}(2)				±1	µA
I_{IN}(3)				+100	µA
Output Logic Level:					
V_{OH}(4)	I_{OH} = –1.6mA	4.5			V
V_{OL}(4)	I_{OL} = +3.2mA			0.5	V
Sampling Frequency		4	44.1	48	kHz
System Clock Frequency	256f_S	1.024	11.2896	12.2880	MHz
	384f_S	1.536	16.9344	18.4320	MHz
	512f_S	2.024	22.5792	24.5760	MHz
DC ACCURACY					
Gain Mismatch Channel-to-Channel			±1.0	±2.5	% of FSR
Gain Error			±2.0	±5.0	% of FSR
Gain Drift			±20		ppm of FSR/°C
Bipolar Zero Error	High-Pass Filter Bypass		±2.0		% of FSR
Bipolar Zero Drift	High-Pass Filter Bypass		±20		ppm of FSR/°C
DYNAMIC PERFORMANCE(5)					
THD+N at FS (–0.5dB)			–88	–80	dB
THD+N at –60dB			–90		dB
Dynamic Range	EIAJ, A-weighted	90	93		dB
Signal-To-Noise Ratio	EIAJ, A-weighted	90	93		dB
Channel Separation		88	91		dB
ANALOG INPUT					
Input Range	FS (V_{IN} = 0dB)		2.828		Vp-p
Center Voltage			2.1		V
Input Impedance			30		kΩ
Anti-Aliasing Filter Frequency Response	–3dB		170		kHz
DIGITAL FILTER PERFORMANCE					
Passband				0.454f_S	Hz
Stopband		0.583f_S			Hz
Passband Ripple				±0.05	dB
Stopband Attenuation		–65			dB
Delay Time (Latency)			17.4/f_S		sec
High Pass Frequency Response	–3dB			0.019f_S	mHz
POWER SUPPLY REQUIREMENTS					
Voltage Range	$+V_{CC}$	+4.5	+5.0	+5.5	VDC
	$+V_{DD}$	+4.5	+5.0	+5.5	VDC
Supply Current(6)	$+V_{CC}$ = $+V_{DD}$ = +5V		18	25	mA
Power Dissipation	$+V_{CC}$ = $+V_{DD}$ = +5V		90	125	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+125	°C
Thermal Resistance, θ_{JA}			100		°C/W

NOTES: (1) Pins 5, 6, 7, 9, and 10 (SCKI, BCK, LRCK, BYPAS, FMT). (2) Pins 5, 6, 7 (SCKI, BCK, LRCK) Schmitt-Trigger input. (3) Pins 9, 10 (BYPAS, FMT) Schmitt-Trigger input with 100kΩ typical pull-down resistor). (4) Pin 8 (DOUT). (5) f_{IN} = 1kHz, using Audio Precisions System II, rms Mode with 20kHz LPF and 400Hz HPF enabled. (6) No load on DOUT (pin 8).

PIN CONFIGURATION

Top View **SOIC**



PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	$V_{IN}L$	IN	Analog Input, Lch.
2	$V_{IN}R$	IN	Analog Input, Rch.
3	DGND	—	Digital Ground
4	V_{DD}	—	Digital Power Supply
5	SCKI	IN	System Clock Input; $256f_S$, $384f_S$, or $512f_S$.
6	BCK	IN	Bit Clock Input
7	LRCK	IN	Sampling Clock Input
8	DOUT	OUT	Audio Data Output
9	BYPAS	IN	HPF Bypass Control(1) L: HPF Enabled H: HPF Disabled
10	FMT	IN	Audio Data Format(1) L: MSB-First, Left-Justified H: MSB-First, I^2S
11	V_{CC}	—	Analog Power Supply
12	AGND	—	Analog Ground
13	$V_{REF}2$	—	Reference 2 Decoupling Capacitor
14	$V_{REF}1$	—	Reference 1 Decoupling Capacitor

NOTE: (1) With 100kΩ typical pull-down resistor.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage: $+V_{DD}$, $+V_{CC}$	+6.5V
Supply Voltage Differences	±0.1V
GND Voltage Differences	±0.1V
Digital Input Voltage	–0.3V to (V_{DD} + 0.3V)
Analog Input Voltage	–0.3V to (V_{CC} + 0.3V)
Input Current (any pin except supplies)	±10mA
Power Dissipation	300mW
Operating Temperature Range	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
(reflow, 10s)	+235°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

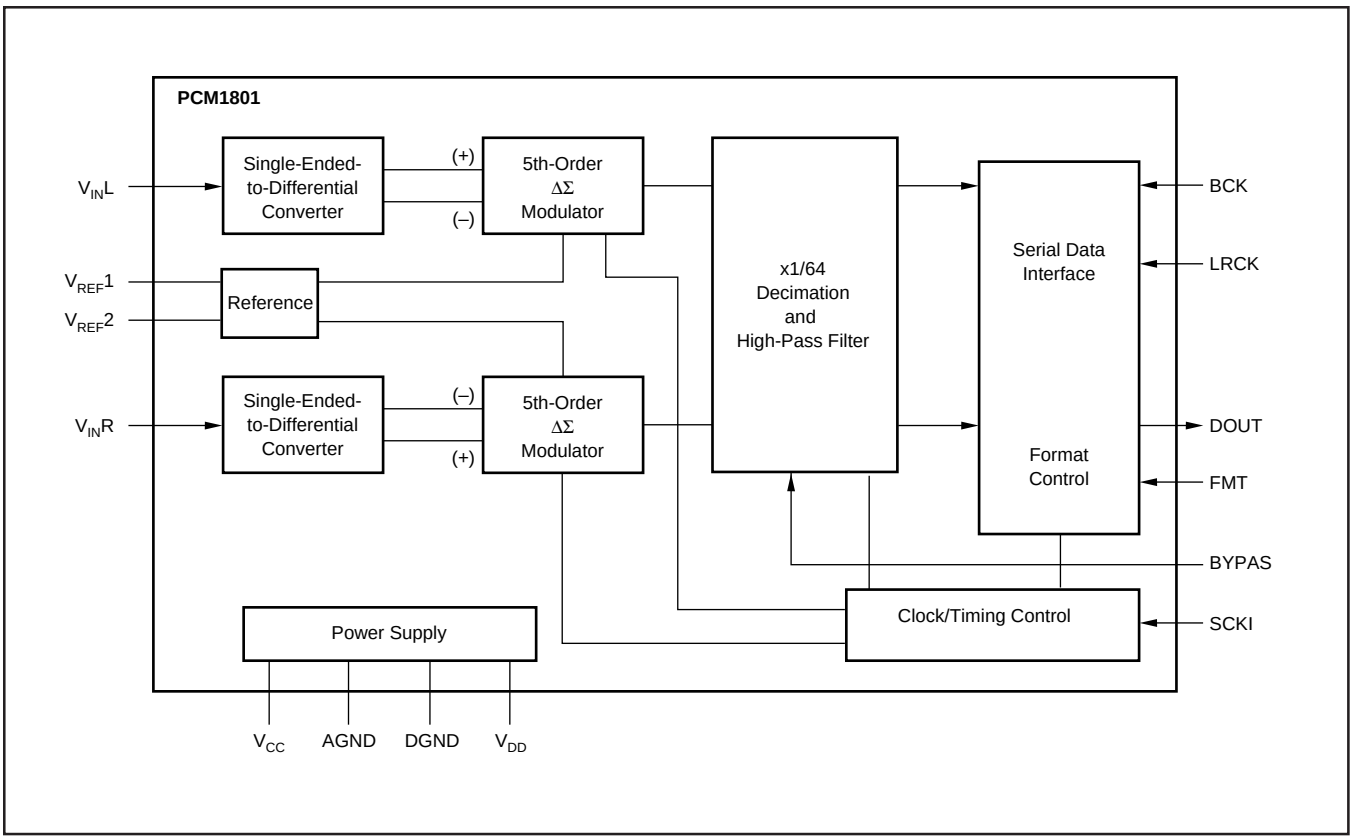
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

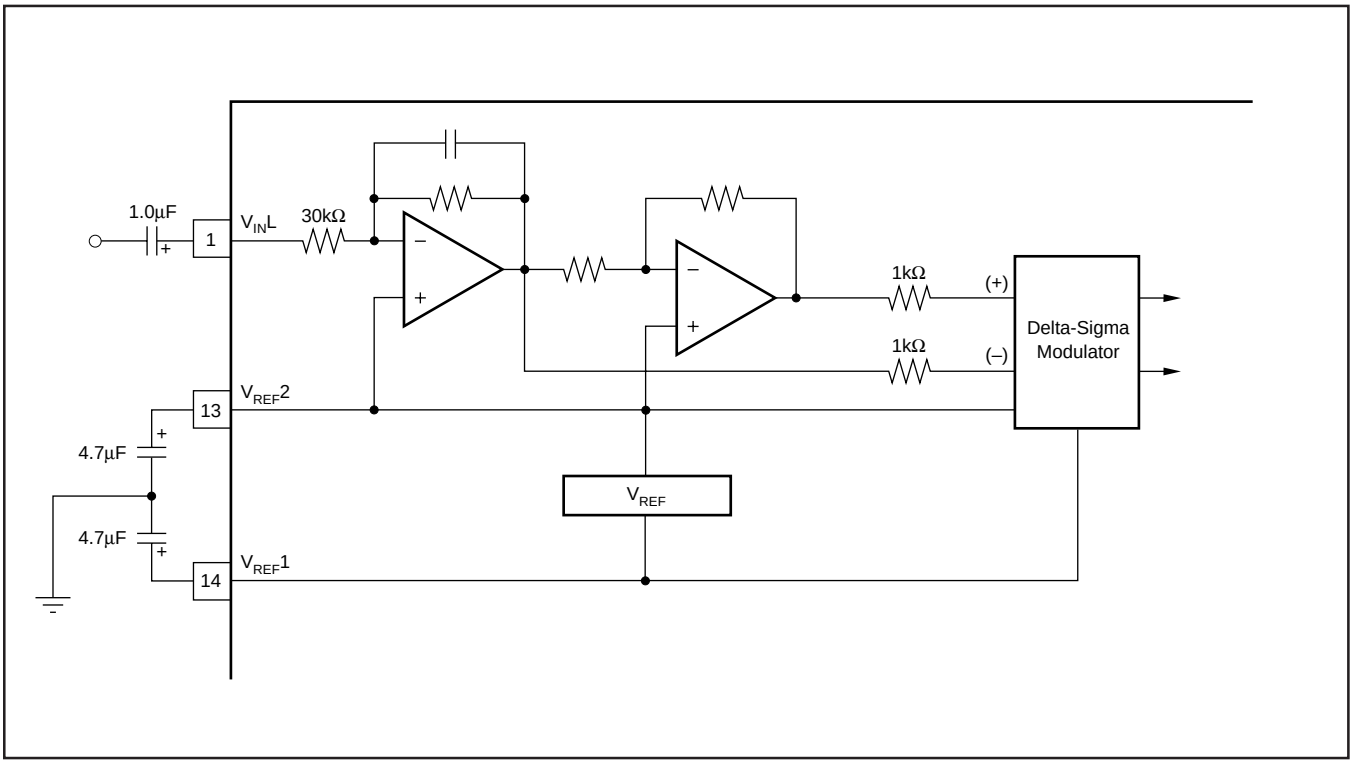
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
PCM1801U	SO-14	235	–25°C to +85°C	PCM1801U	PCM1801U	Rails
"	"	"	"	"	PCM1801U/2K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "PCM1801U/2K" will get a single 2000-piece Tape and Reel.

BLOCK DIAGRAM



ANALOG FRONT-END (Single-Channel)

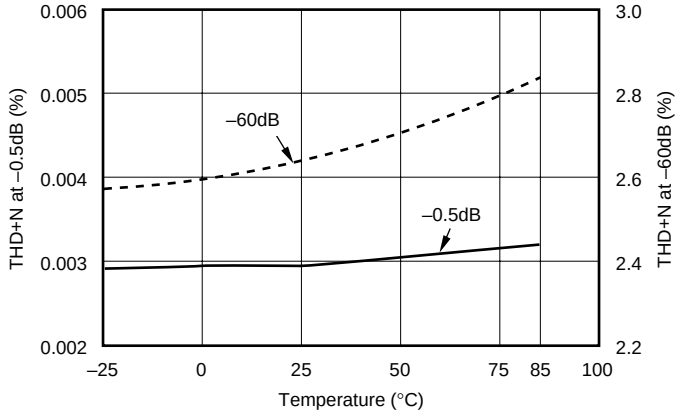


TYPICAL PERFORMANCE CURVES

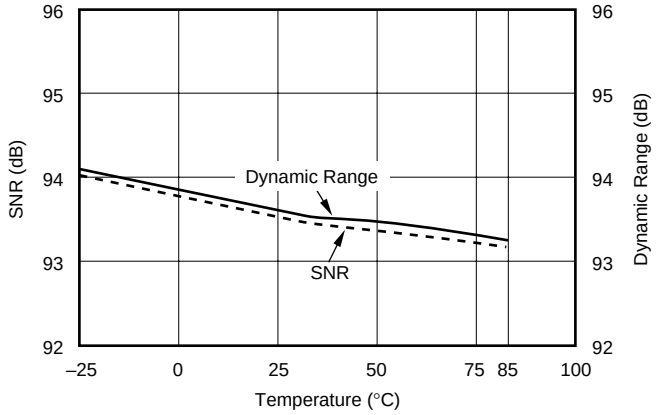
At T_A = +25°C, $+V_{DD}$ = $+V_{CC}$ = +5V, f_S = 44.1kHz, and SYSCLK = 384f_S, unless otherwise noted.

ANALOG DYNAMIC PERFORMANCE

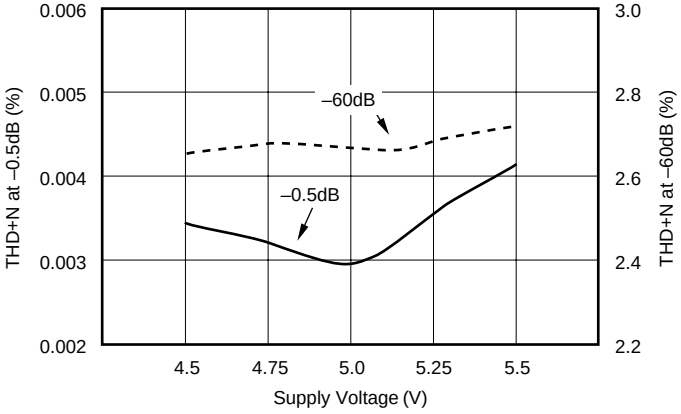
TOTAL HARMONIC DISTORTION + NOISE
vs TEMPERATURE



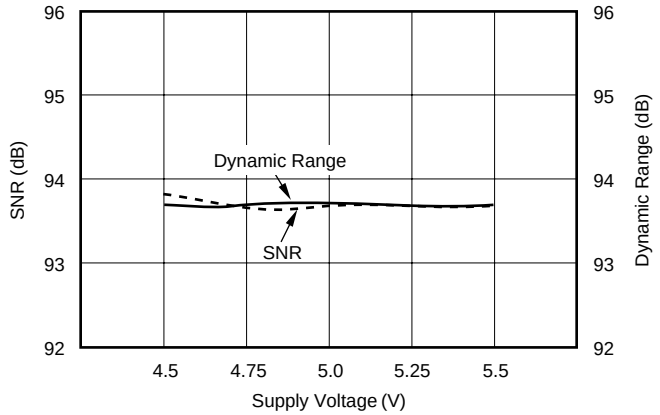
SIGNAL-TO-NOISE RATIO AND DYNAMIC RANGE
vs TEMPERATURE



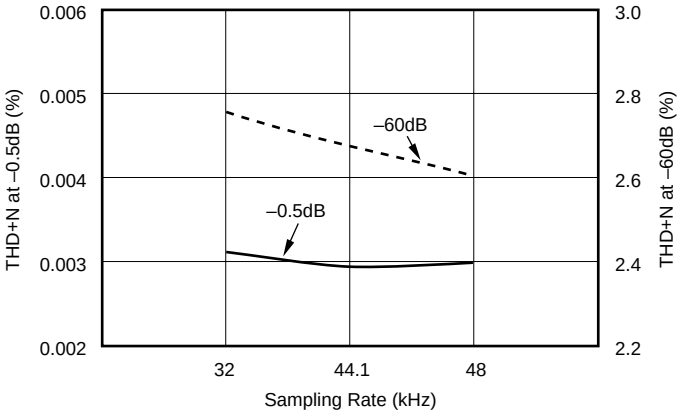
TOTAL HARMONIC DISTORTION + NOISE
vs SUPPLY VOLTAGE



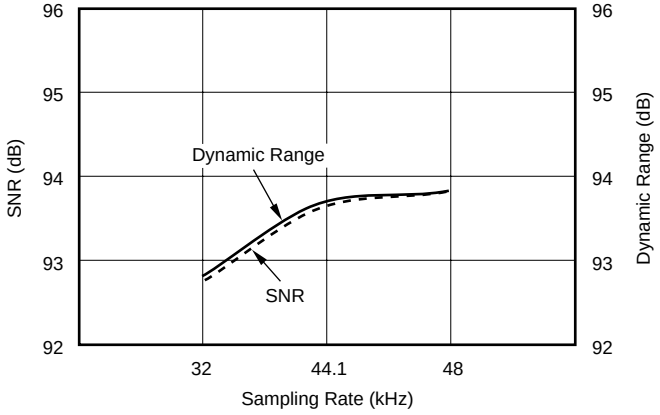
SIGNAL-TO-NOISE RATIO AND DYNAMIC RANGE
vs SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION + NOISE
vs SAMPLING RATE



SIGNAL-TO-NOISE RATIO AND DYNAMIC RANGE
vs SAMPLING RATE

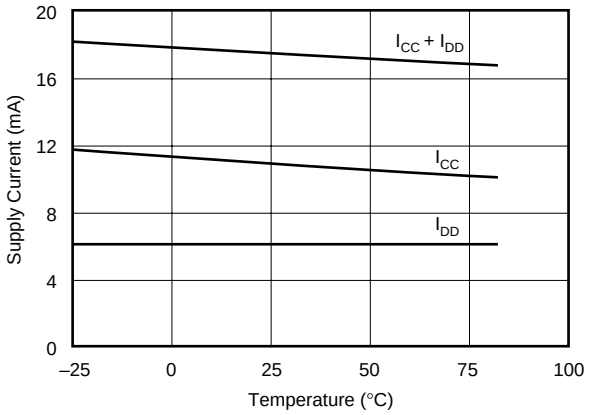


TYPICAL PERFORMANCE CURVES (Cont.)

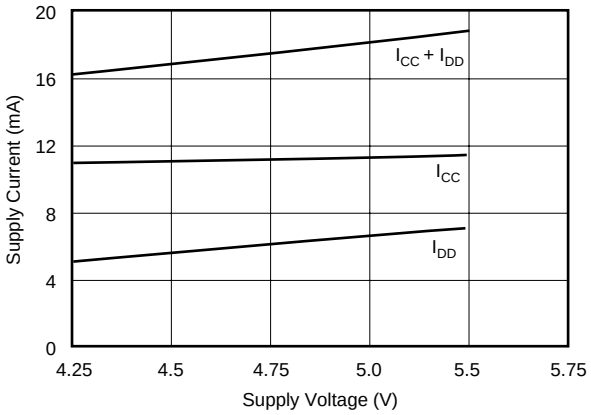
At T_A = +25°C, $+V_{DD}$ = $+V_{CC}$ = +5V, f_S = 44.1kHz, and SYSCLK = 384f_S, unless otherwise noted.

ANALOG DYNAMIC PERFORMANCE (cont.)

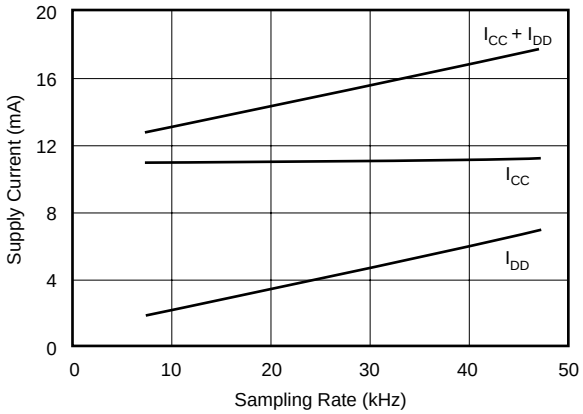
SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs SAMPLING RATE

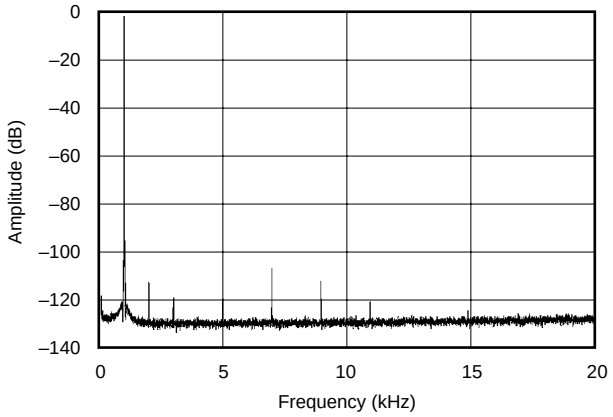


TYPICAL PERFORMANCE CURVES (Cont.)

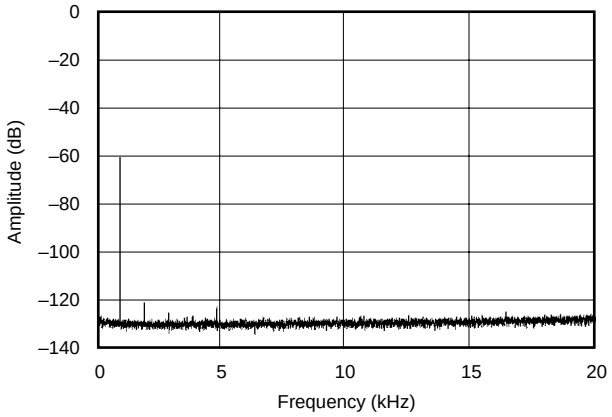
At T_A = +25°C, $+V_{DD}$ = $+V_{CC}$ = +5V, f_S = 44.1kHz, and SYSCLK = 384f_S, unless otherwise noted.

OUTPUT SPECTRUM

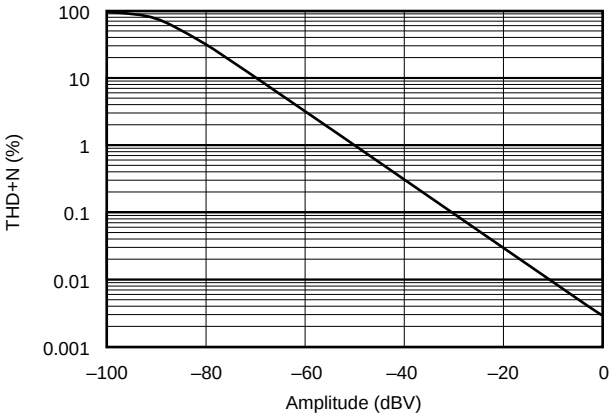
Full-Scale FFT



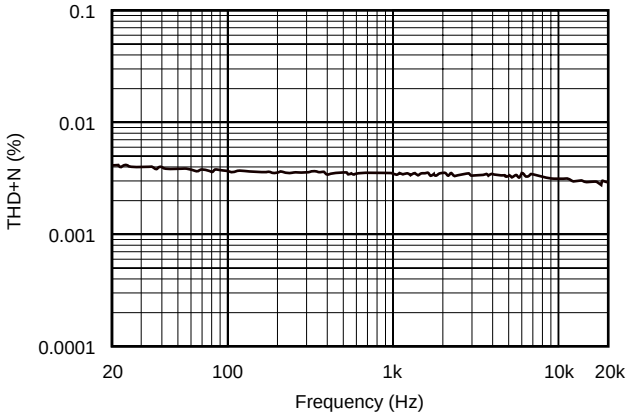
–60dBFS FFT



TOTAL HARMONIC DISTORTION + NOISE
vs AMPLITUDE



TOTAL HARMONIC DISTORTION + NOISE
vs FREQUENCY

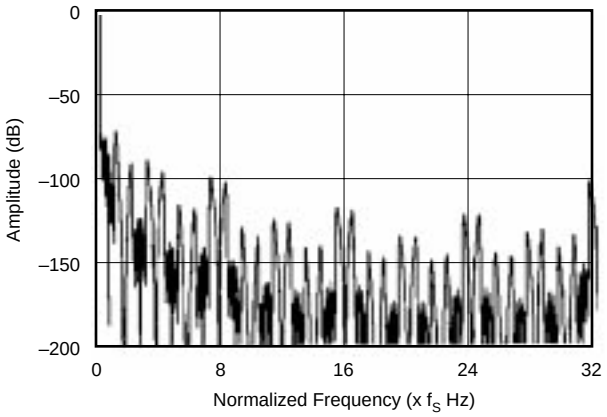


TYPICAL PERFORMANCE CURVES (Cont.)

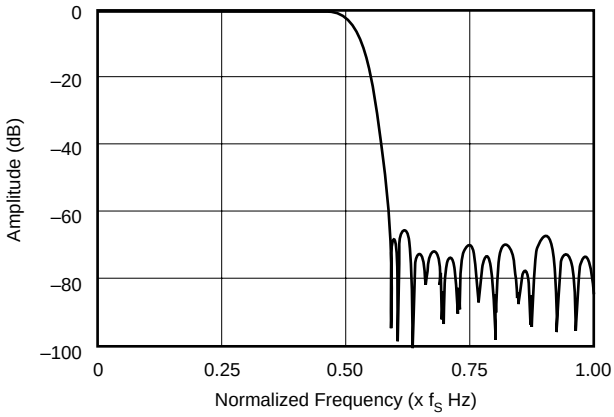
At T_A = +25°C, $+V_{DD}$ = $+V_{CC}$ = +5V, f_S = 44.1kHz, and SYSCLK = 384f_S, unless otherwise noted.

DIGITAL FILTER

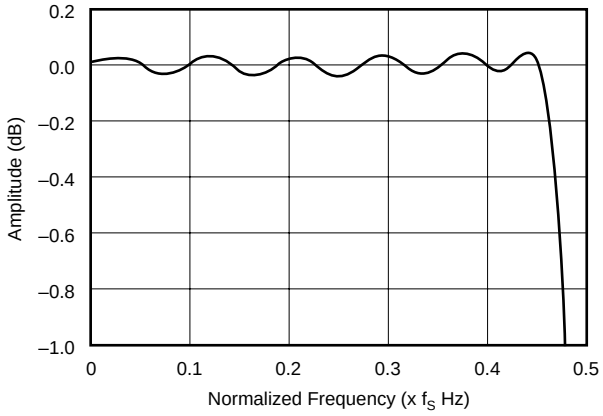
OVERALL CHARACTERISTICS



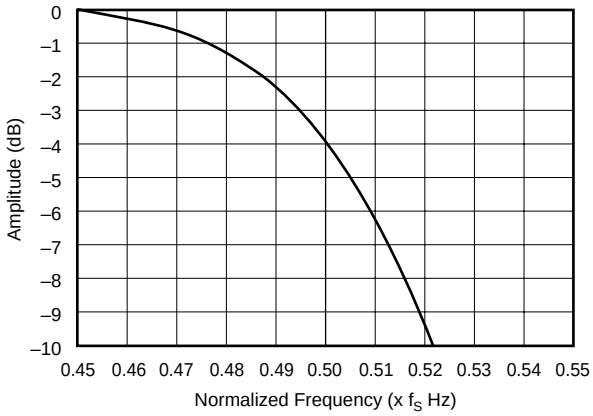
STOPBAND ATTENUATION CHARACTERISTICS



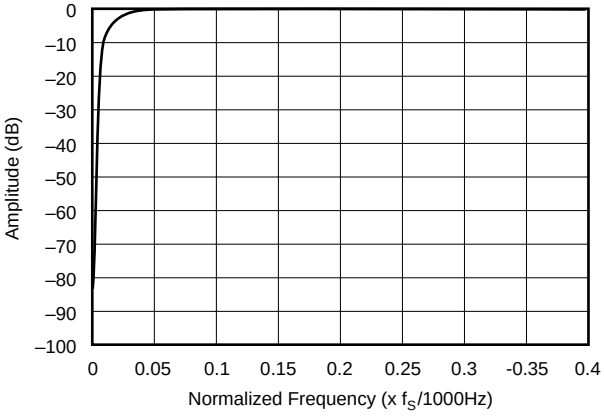
PASSBAND RIPPLE CHARACTERISTICS



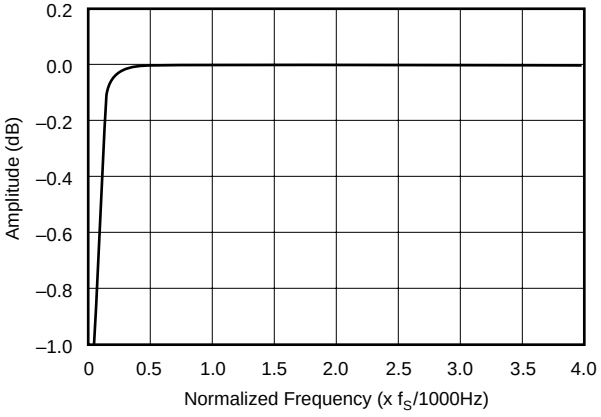
TRANSITION BAND CHARACTERISTICS



HIGH PASS FILTER RESPONSE



HIGH PASS FILTER RESPONSE

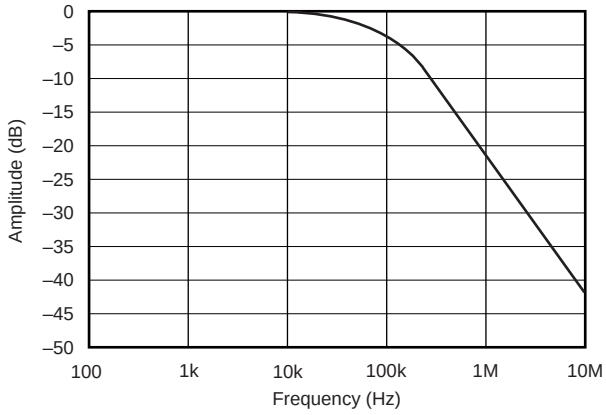


TYPICAL PERFORMANCE CURVES (Cont.)

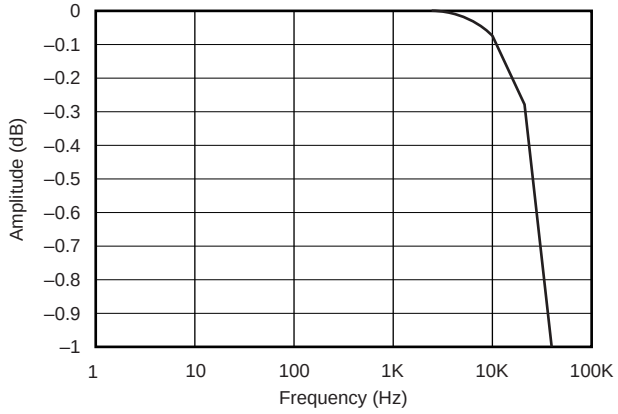
At T_A = +25°C, $+V_{DD}$ = $+V_{CC}$ = +5V, f_S = 44.1kHz, and SYSCLK = 384f_S, unless otherwise noted.

ANTI-ALIASING

ANTI-ALIASING FILTER
STOPBAND FREQUENCY RESPONSE



ANTI-ALIASING FILTER
PASSBAND FREQUENCY RESPONSE



THEORY OF OPERATION

PCM1801 consists of a bandgap reference, two channels of a single-to-differential converter, a fully differential 5th-order delta-sigma modulator, a decimation filter (including digital high pass), and a serial interface circuit. The Block Diagram illustrates the total architecture of PCM1801, the Analog Front-End diagram illustrates the architecture of the single-to-differential converter, and the anti-aliasing filter is illustrated in the Block Diagram. Figure 1 illustrates the architecture of the 5th-order delta-sigma modulator and transfer functions.

An internal high precision reference with two external capacitors provides all reference voltages which are required by the converter, and defines the full-scale voltage range of both channels. The internal single-ended to differential voltage converter saves the design, space and extra parts needed for external circuitry required by many delta-sigma converters. The internal full differential architecture provides a wide dynamic range and excellent power supply rejection performance.

The input signal is sampled at 64x oversampling rate, eliminating the need for a sample-and-hold circuit, and simplifying anti-alias filtering requirements. The 5th-order delta-sigma noise shaper consists of five integrators which use a switched-capacitor topology, a comparator and a feedback loop consisting of a 1-bit DAC. The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels.

The $64f_S$, 1-bit stream from the modulator is converted to $1f_S$, 16-bit digital data by the decimation filter, which also acts as a low-pass filter to remove the shaped quantization noise. The DC components are removed by a digital high-pass filter, and the filtered output is converted to time-multiplexed serial signals through a serial interface which provides flexible serial formats.

SYSTEM CLOCK

The system clock for PCM1801 must be either $256f_S$, $384f_S$, or $512f_S$, where f_S is the audio sampling frequency. The system clock must be supplied on SCKI (pin 5).

PCM1801 also has a system clock detection circuit which automatically senses if the system clock is operating at $256f_S$, $384f_S$, or $512f_S$.

When $384f_S$ and $512f_S$ system clock are used, the PCM1801 automatically divides these clocks down to $256f_S$ internally. This $256f_S$ clock is used to operate the digital filter and the modulator. Table I lists the relationship of typical sampling frequencies and system clock frequencies. Figure 2 illustrates the system clock timing.

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)		
	$256f_S$	$384f_S$	$512f_S$
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9340	22.5792
48	12.2880	18.4320	24.5760

TABLE I. System Clock Frequencies.

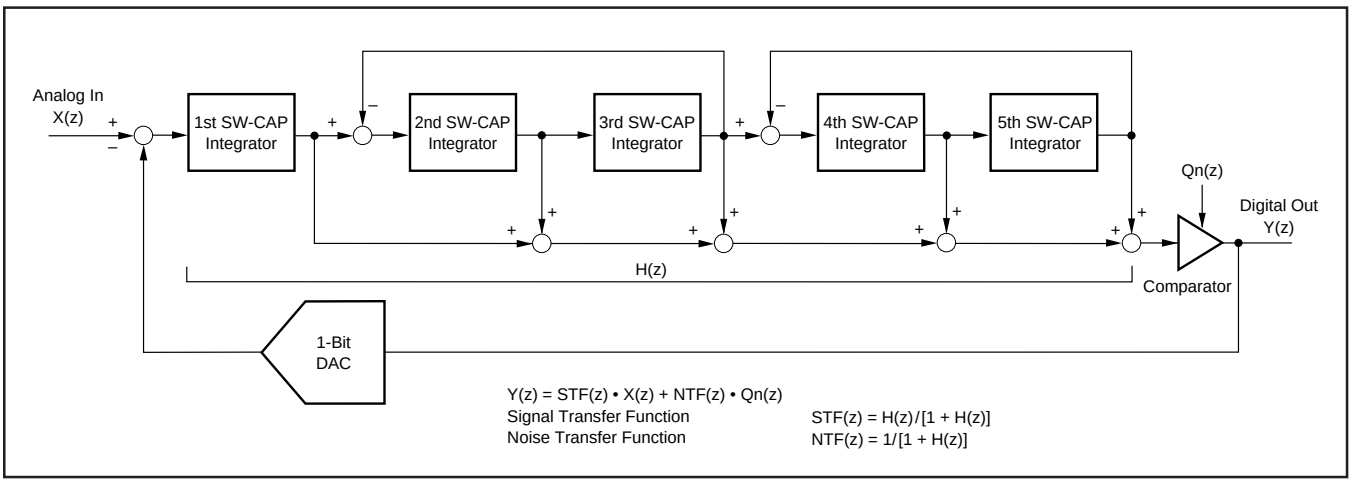


FIGURE 1. Simplified Diagram of the PCM1801 5th-Order Delta-Sigma Modulator.

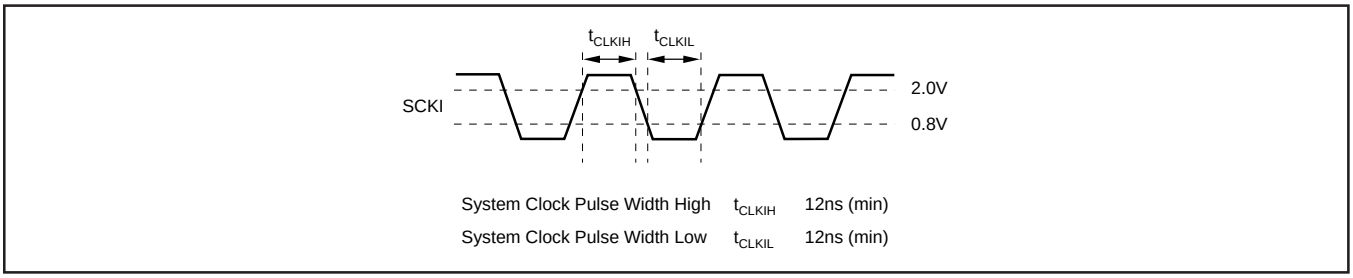


FIGURE 2. System Clock Timing.

RESET

PCM1801 has an internal power-on reset circuit, which initializes (resets) when the supply voltage (V_{CC}/V_{DD}) exceeds 4.0V (typ). The PCM1801 stays in the reset state and the digital output is forced to zero. The digital output is valid after reset state release and $18436f_S$ periods. During reset, the logic circuits and the digital filter stop operating. Figure 3 illustrates the internal power-on reset timing.

SERIAL AUDIO DATA INTERFACE

The PCM1801 interfaces the audio system through BCK (pin 6), LRCK (pin 7), and DOUT (pin 8).

DATA FORMAT

PCM1801 supports two audio data formats in Slave Mode, and are selected by the FMT control input (pin 10) as shown in Table II.

FMT	DATA FORMAT
0 (L)	16-Bit, Left-Justified
1 (H)	16-Bit, I^2S

TABLE II. Data Format.

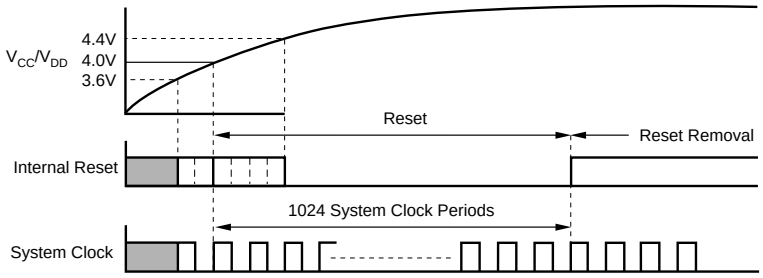


FIGURE 3. Internal Power-On Reset Timing.

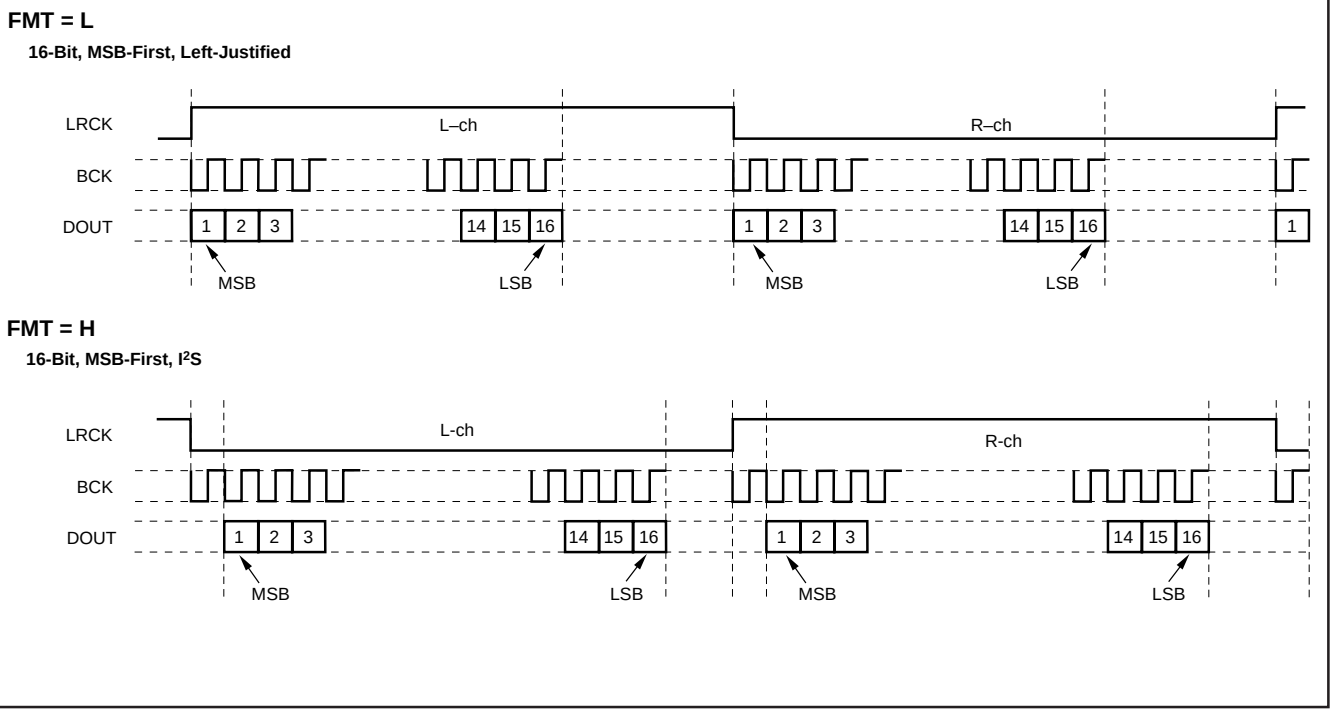


FIGURE 4. Audio Data Format (Slave Mode: LRCK, and BCK are inputs).

SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM

PCM1801 operates with LRCK synchronized to the system clock (SCKI). PCM1801 does not require a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI. If the relationship between LRCK and SCKI changes more than 6 bit clocks (BCK) during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within $1/f_S$ and the digital output is forced to BPZ until resynchronization between LRCK and SCKI is completed. In case of changes less than 5 bit clocks (BCK), resynchronization does not occur and above digital output control and discontinuity does not occur.

ADC DATA OUTPUT AT RESET

Figures 6 and 7 illustrate the ADC digital output for the reset operation and loss of synchronization state. During undefined data, it may generate some noise in the audio signal. Also, the transition of normal to undefined data and undefined or zero data to normal makes a discontinuity of data on the digital output, and may generate some noise in the audio signal.

BOARD DESIGN AND LAYOUT CONSIDERATIONS

V_{CC}, V_{DD} PINS

The digital and analog power supply lines to the PCM1801 should be bypassed to the corresponding ground pins with both 0.1µF and 10µF capacitors as close to the pins as possible to maximize the dynamic performance of the ADC. Although PCM1801 has two power lines to maximize the potential of dynamic performance, using one common power supply is recommended to avoid unexpected power supply problems, such as latch-up due to power supply sequencing.

AGND, DGND PINS

To maximize the dynamic performance of the PCM1801, the analog and digital grounds are not internally connected. These points should have very low impedance to avoid digital noise feedback into the analog ground. They should be connected directly to each other under the PCM1801 package to reduce potential noise problems.

V_{IN} PINS

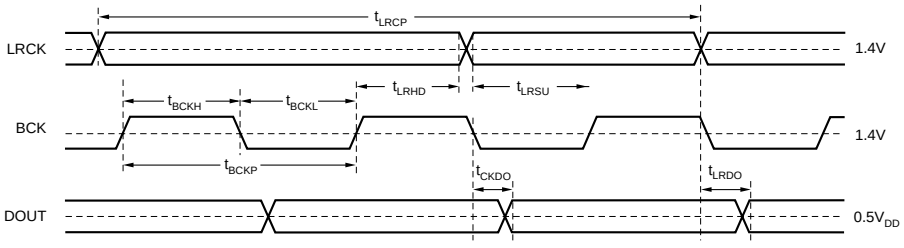
A 1.0µF tantalum capacitor is recommended as an AC-coupling capacitor which establishes a 5.3Hz cut-off frequency. If a higher full-scale input voltage is required, the input voltage range can be increased by adding a series resistor to the V_{IN} pins.

V_{REF} INPUTS

A 4.7µF tantalum capacitor is recommended between ground and the $V_{REF}1$ and $V_{REF}2$ references to ensure low source impedance. These capacitors should be located as close as possible to the $V_{REF}1$ or $V_{REF}2$ pins to reduce dynamic errors on the ADC's references.

SYSTEM CLOCK

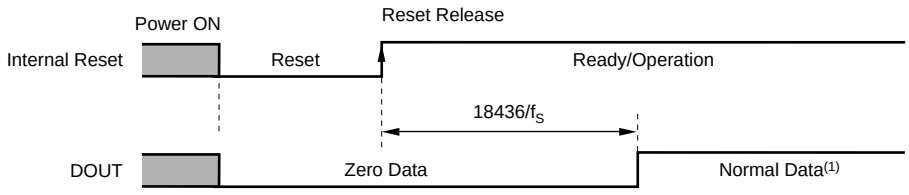
The quality of the system clock can influence dynamic performance in the PCM1801. The duty cycle, jitter, and threshold voltage at the system clock input pin must be carefully managed. When power is supplied to the part, the system clock, bit clock (BCK), and word clock (LRCK) should also be supplied simultaneously. Failure to supply the audio clocks will result in a power dissipation increase of up to three times normal dissipation and may degrade long-term reliability if the maximum power dissipation limit is exceeded.



DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNITS
BCK Period	t_{BCKP}	300			ns
BCK Pulse Width HIGH	t_{BCKH}	120			ns
BCK Pulse Width LOW	t_{BCKL}	120			ns
LRCK Set Up Time to BCK Rising Edge	t_{LRSU}	80			ns
LRCK Hold Time to BCK Rising Edge	t_{LRHD}	40			ns
LRCK Period	t_{LRCP}	20			µs
Delay Time BCK Falling Edge to DOUT Valid	t_{CKDO}	–20		40	ns
Delay Time LRCK Edge to DOUT Valid	t_{LRDO}	–20		40	ns
Rising Time of All Signals	t_{RISE}			20	ns
Falling Time of All Signals	t_{FALL}			20	ns

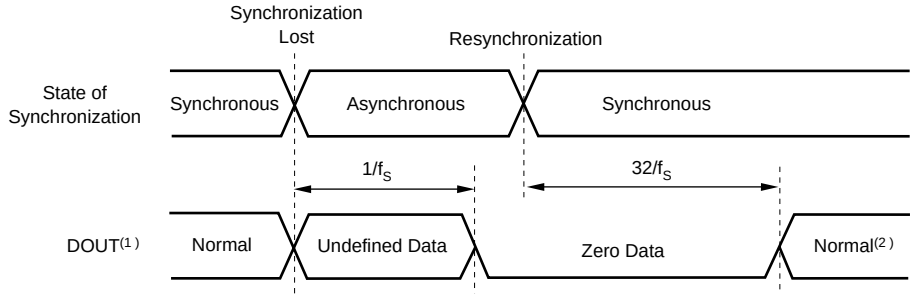
NOTE: Timing measurement reference level is $(V_{IH}/V_{IL})/2$. Rising and falling time is measured from 10% to 90% of I/O signals' swing. Load capacitance of DOUT signal is 20pF.

FIGURE 5. Audio Data Interface Timing (LRCK and BCK are inputs).



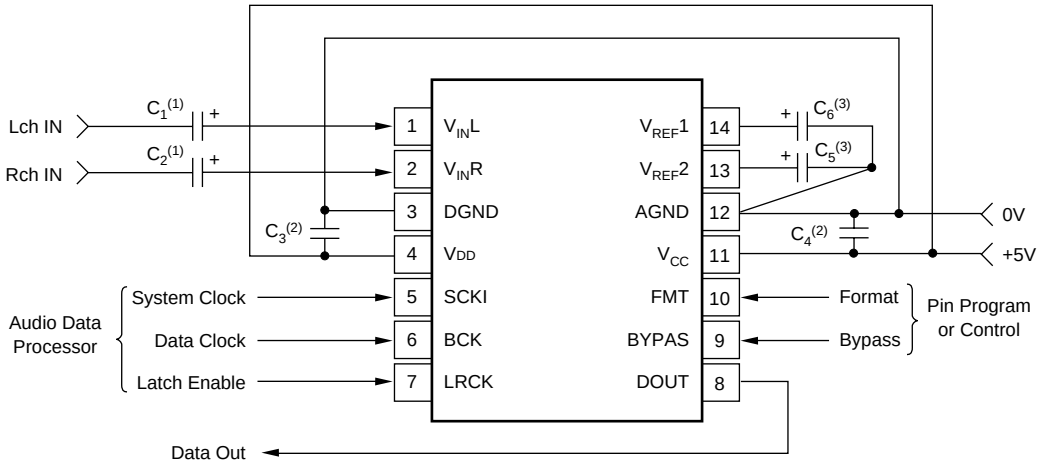
NOTE: (1) The HPF transient response (exponentially attenuationed signal from ±0.2% DC of FSR with 200ms time constant) appears initially.

FIGURE 6. ADC Output for Power-On Reset and RSTB Control.



NOTES: (1) Applies only for Slave Mode—the loss of synchronization never occurs in Master Mode.
(2) The HPF transient response (exponentially attenuationed signal from ±0.2% DC of FSR with 200ms time constant) appears initially.

FIGURE 7. ADC Output for Loss of Synchronization.



NOTES: (1) C_1 and C_2: A 1µF capacitor gives 5.3Hz (τ = 1µF * 30kΩ) cut-off frequency for input HPF in normal operation and requires power-on setting time of 6ms at power up.
(2) C_3 and C_4: Bypass capacitor 0.1µF ceramic and 10µF tantalum or aluminum electrolytic, depending on layout and power supply.
(3) C_5 and C_6: 4.7µF tantalum or aluminum electrolytic capacitor.

FIGURE 8. Typical Circuit Connection.