ESP8266

System Description

Version 1.4

About This Guide

This document provides technical description of ESP8266 series products including ESP8266EX, ESP-LAUNCHER, and ESP-WROOM, including the following topics:

Chapter	Title	Subject
Chapter 1	ESP8266EX	Provides hardware description on ESP8266EX chipset including.technical specifications, pin definitions, layout, and typical applications.
Chapter 2	ESP-LAUNCHER	Provides technical description on ESP-LAUNCHER with ESP8266EX built-in.
Chapter 3	ESP-WROOM	Provides technical description on ESP-WROOM-01 and ESP-WROOM-02 with ESP8266EX chipset.

Release Notes

Date	Version	Release notes
2015.12	V1.3	First release.
2016.01	V1.4	Sections 1.5.2, 1.5.3 & 1.6 updated.

Table of Contents

1. ESP8266EX

1.1. Overview

Espressif's ESP8266EX delivers highly integrated Wi-Fi SoC solution to meet the continuous demands for efficient power usage, compact design and reliable performance in the industry.

With the complete and self-contained Wi-Fi networking capabilities, It can perform as either a standalone application or the slave to a host MCU. When ESP8266EX hosts the application, it promptly boots up from the external flash. The integrated high-speed cache helps to increase the system performance and optimise the system memory. Also, ESP8266EX can be applied to any micro-controller design as a Wi-Fi adaptor through SPI / SDIO or I2C / UART interfaces.

ESP8266EX integrates antenna switches, RF balun, power amplifier, low noise receive amplifier, filters and power management modules. The compact design minimise the PCB size and allows for minimal external circuitry.

Besides the Wi-Fi functionalities, ESP8266EX also integrates an enhanced version of Tensilica's L106 Diamond series 32-bit processor and on-chip SRAM. It can be interfaced with external sensors and other devices through the GPIOs. Software Development Kit (SDK) provides sample codes for various applications.

Espressif Systems' Smart Connectivity Platform (ESCP) enables sophisticated features include fast switching between sleep and wake-up mode for energy-efficiency purpose, adaptive radio biasing for low-power operation, advance signal processing, spur cancellation and radio co-existence mechanisms for common cellular, Bluetooth, DDR, LVDS, LCD interference mitigation.

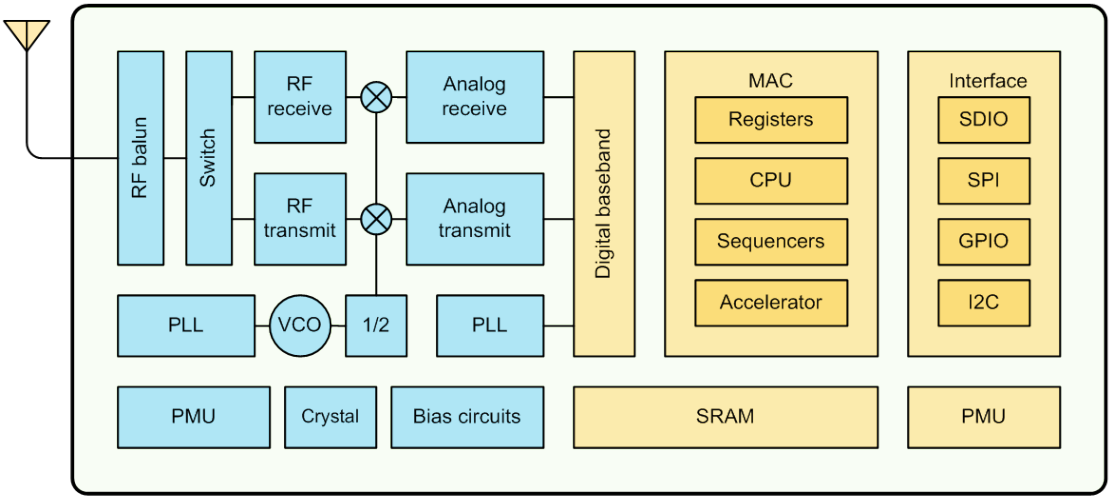


Figure 1-1: ESP8266EX block diagram

1.2. Specifications

Table 1-1: ESP8266EX specifications

Categories	Items	Parameters
Wi-Fi	Standard	CCC / FCC / CE / TELEC / SRRC
	Protocols	802.11 b/g/n
	Frequency Range	2.4 G ~ 2.5 G (2400 M ~ 2483.5 M)
	Tx power	802.11 b: +20 dBm
		802.11 g: +17 dBm
		802.11 n: +14 dBm
	Rx Sensitivity	802.11 b: -91 dbm (11 Mbps)
		802.11 g: -75 dbm (54 Mbps)
		802.11 n: -72 dbm (MCS7)
	Antenna	PCB trace, external, IPEX connector, ceramic chip
Hardware	Peripheral interface	UART / SDIO / SPI / I2C / I2S / IR Remote Control
		GPIO / PWM
	Operating voltage	3.0 V ~ 3.6 V
	Operating current	Average: 80mA
	Operating temperature range	-40 ℃ ~ 125 ℃
	Storage temperature range	-40 ℃ ~ 125 ℃
	Package size	QFN32-pin (5 mm x 5 mm)
	External interface	N/A
Software	Wi-Fi mode	station / softAP / SoftAP + station
	Security	WPA / WPA2
	Encryption	WEP / TKIP / AES
	Firmware upgrade	UART Download / OTA (via network)
	Software development	SDK for customised development / cloud server development
	Network Protocols	IPv4, TCP / UDP / HTTP / FTP
	User configuration	AT Instruction Set, Cloud Server, Android/ iOS App

1.3. Pin Definitions

The pin assignments for 32-pin QFN package is illustrated in Figure 1-2.

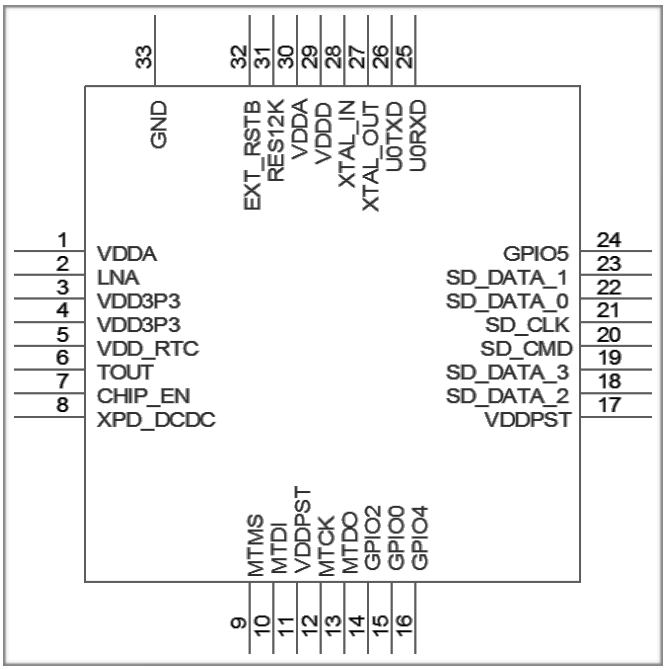


Figure 1-2: ESP8266EX pin assignments

Table 1-2 lists the definitions and functions of each pin.

Table 1-2: ESP8266EX pin definitions

Pin	Name	Type	Functions
1	VDDA	P	Analog Power 3.0 V ~ 3.6V
2	LNA	I/O	RF Antenna Interface Chip Output Impedance = 50 Ω No matching required. It is suggested to retain the π-type matching network to match the antenna.
3	VDD3P3	P	Amplifier power: 3.0 V ~ 3.6 V
4	VDD3P3	P	Amplifier power:3.0 V ~ 3.6 V
5	VDD_RTC	P	NC (1.1 V)
6	TOUT	I	ADC pin. It can be used to test the power-supply voltage of VDD3P3 (Pin3 and Pin4) and the input power voltage of TOUT (Pin 6). However, these two functions cannot be used simultaneously.
7	CHIP_EN	I	Chip Enable High: On, chip works properly Low: Off, small current consumed
8	XPD_DCDC	I/O	Deep-sleep wakeup (need to be connected to EXT_RSTB; GPIO16
9	MTMS	I/O	GPIO14; HSPI_CLK

Pin	Name	Type	Functions
10	MTDI	I/O	GPIO12; HSPI_MISO
11	VDDPST	P	Digital / IO power supply (1.8 V ~ 3.3 V)
12	MTCK	I/O	GPIO13; HSPI_MOSI; UART0_CTS
13	MTDO	I/O	GPIO15; HSPI_CS; UART0_RTS
14	GPIO2	I/O	UART Tx during flash programming; GPIO2
15	GPIO0	I/O	GPIO0; SPI_CS2
16	GPIO4	I/O	GPIO4
17	VDDPST	P	Digital / IO power supply (1.8 V ~ 3.3 V)
18	SDIO_DATA_2	I/O	Connect to SD_D2 (Series R: 200 Ω); SPIHD; HSPIHD; GPIO9
19	SDIO_DATA_3	I/O	Connect to SD_D3 (Series R: 200 Ω); SPIWP; HSPIWP; GPIO10
20	SDIO_CMD	I/O	Connect to SD_CMD (Series R: 200 Ω); SPI_CS0; GPIO11
21	SDIO_CLK	I/O	Connect to SD_CLK (Series R: 200 Ω); SPI_CLK; GPIO6
22	SDIO_DATA_0	I/O	Connect to SD_D0 (Series R: 200 Ω); SPI_MSIO; GPIO7
23	SDIO_DATA_1	I/O	Connect to SD_D1 (Series R: 200 Ω); SPI_MOSI; GPIO8
24	GPIO5	I/O	GPIO5
25	U0RXD	I/O	UART Rx during flash programming; GPIO3
26	U0TXD	I/O	UART Tx during flash programming; GPIO1; SPI_CS1
27	XTAL_OUT	I/O	Connect to crystal oscillator output, can be used to provide BT clock input
28	XTAL_IN	I/O	Connect to crystal oscillator input
29	VDDD	P	Analog power 3.0 V ~ 6 V
30	VDDA	P	Analog power 3.0 V ~ 3.6 V
31	RES12K	I	Serial connection with a 12 kΩ resistor to the ground
32	EXT_RSTB	I	External reset signal (Low voltage level: Active)

Note :

GPIO2, GPIO0 and MTDO can be configurable as 3-bit SDIO mode.

1.4. Schematics

The highly integrated design of ESP8266EX chipset tremendously reduce the number of components required. Beside ESP8266EX, less than ten resistors and capacitors, one crystal oscillator and one SPI flash are needed to make a complete module with wireless communication capability.

The complete circuit diagram of ESP8266EX is illustrated in Figure 1-3.

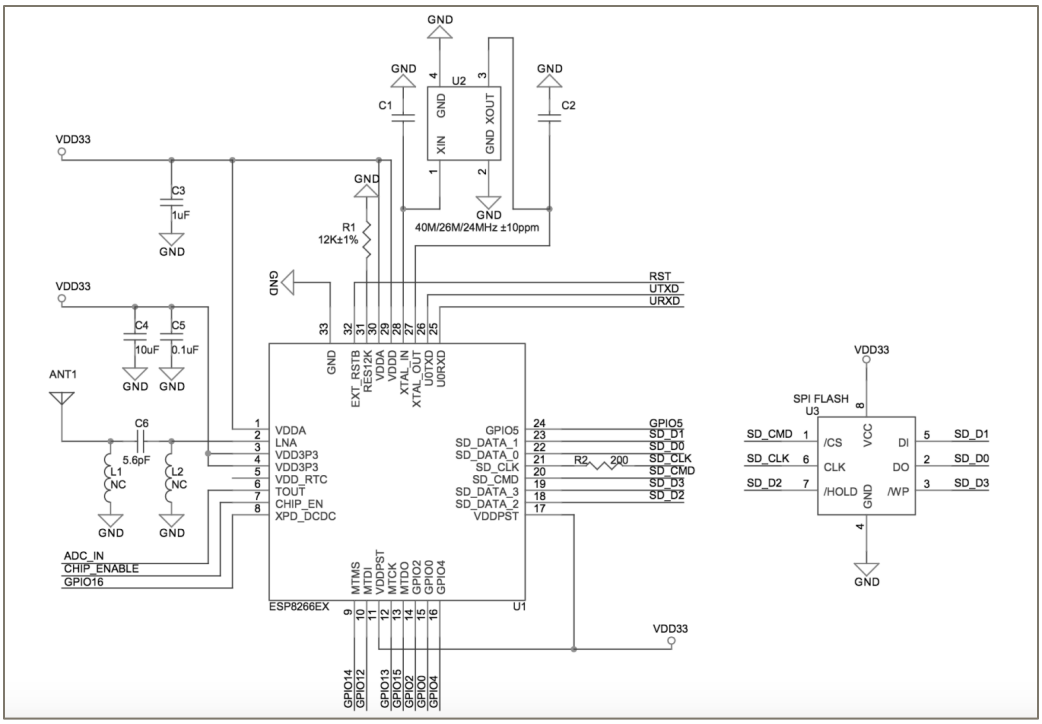


Figure 1-3: ESP8266EX schematics

ESP8266EX schematics design includes six aspects:

- Power supply
- Power-on sequence and reset
- Flash
- Crystal oscillator
- RF
- External resistor

1.4.1. Power Supply

Digital Power Supply

ESP8266EX has two digital pins for power supply, pin11 and pin17. For digital power supply, there is no need to add additional filter capacitors. The operating voltage range of digital power supply pins is 1.8 V ~ 3.3 V.

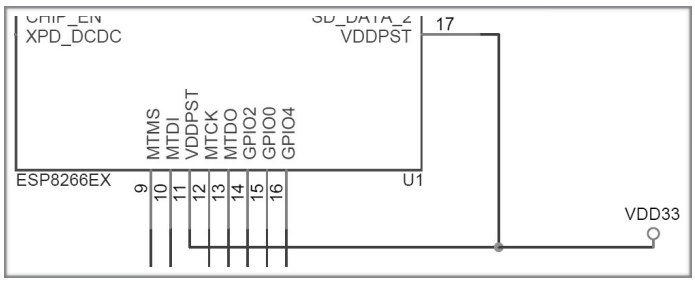


Figure 1-4: ESP8266EX digital power supply pins

Analog power supply

ESP8266EX has five analog pins for power supply. including pin1, pin3, pin4 which provides internal power supply for internal PA and LNA respectively, and pin28, pin29 which supply power for internal PLL. The operating voltage for analog power supply pins is 1.8 V ~ 3.3 V.

It should be noted that the power supply channel might be damaged due to the sudden increase of current when ESP8266EX is transmitting analog signals. Therefore, an additional 0.1uF capacitor with a package size of 0603 or 0805 is needed in circuit design,which can match with capacitor with 0.1uF capacitor with 0402 package.

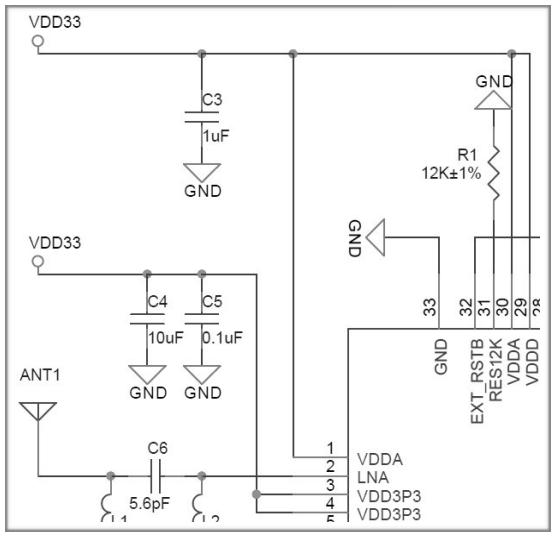


Figure 1-5: ESP8266EX AVDD

Note :
ESP8266EX's EMC is in conformity with FCC and CE requirements, there is no need to add ferrite beads in analog power-supply circuit.

1.4.2. Power-on Sequence and Power Reset

Power-on Sequence

ESP8266EX uses 3.3 V as the system power supply. It is not allowed that Pin7 CH_EN be powered on prior to that the 3.3 V system power supply is powered on.

⚠Notice :

If the power management IC is connected with the power-on enable pin CHIP_EN, it can control the power on-and-off of ESP8266EX by output high and low voltage through its GPIOs. However, pulsed current might be produced at the same time. In order to delay the transmission of pulsed signal and avoid unstable current of CHIP_EN, a RC time-delay circuit (R=1 kΩ, C=100 nF) is needed. There is an internal pull-up in the CHIP_EN pin, so no external pull-up is needed.

Reset

Pin32 serves as a RST pin which can be dangled when it is not used. The reset pin is held low level when the chip is enabled. In order to avoid reset caused by external interference, the lead is generally required to be short, and no external pull-up resistor is necessary.

Pin7 CH_EN can also be used as a reset pin. When the voltage for CH_EN pin is low, the chipset will be powered off.

> ⚠Notice :
>
> Pin 7 CH_EN cannot be dangled.

1.4.3. Flash

The demo flash used by ESP8266EX is SPI Flash with 2 MB ROM in SOIC_8 (SOP_8) package. Pin21 SD_CLK is connected to the Flash CLK pin together with a 0402 resistor in serial connection to reduce the drive current and eliminate external interruption. The initial resistance of the resistor is 200 ohm.

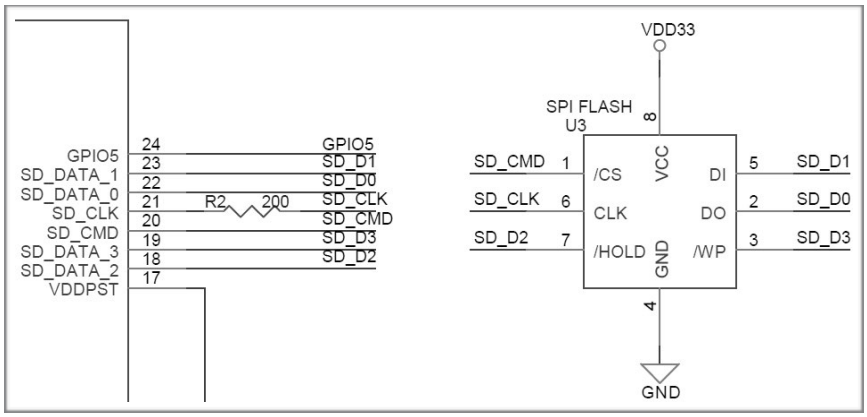


Figure 1-6: ESP8266EX Flash

1.4.4. Crystal Oscillator

40MHz, 26MHz and 24MHz crystal oscillators are supported. The accuracy of crystal oscillators should be ± 10PPM, and the operating temperature range should be between -20°C and 85°C.

Select the corresponding crystal oscillator type in ESP Flash tool. In circuit design, capacitors C1 and C2 which are connected to the earth are added to the input and output terminals of the crystal oscillator respectively. The values of the two capacitors can be flexible, ranging from 6 pF to 22 pF. However, the specific capacitive values of C1 and C2 depend on further testing and adjustment on the overall performance of the whole circuit. Normally, the capacitive values of C1 and C2 are within 10 pF if the crystal oscillator frequency is 26 MHz, while the values of C1 and C2 are 10 pF < C1, C2 < 22 pF if the crystal oscillator frequency is 40 MHz.

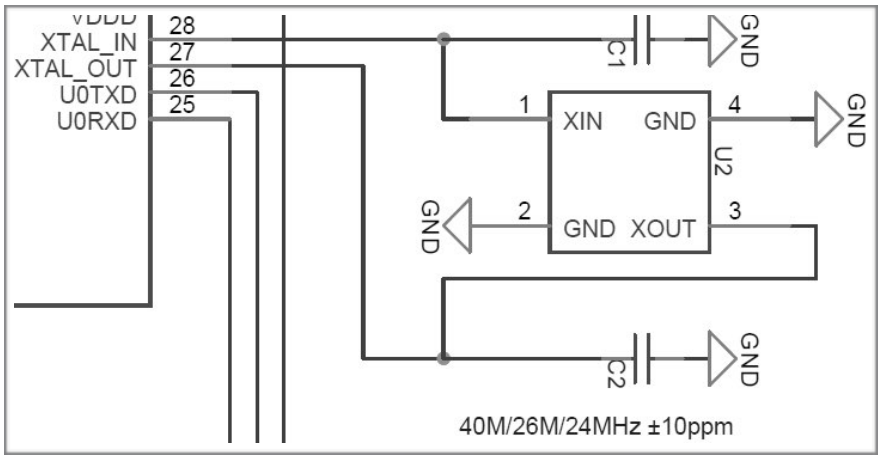


Figure 1-7: ESP8266EX crystal oscillator

⚠Notice :

Defects in the craftsmanship of the crystal oscillators (for example, high frequency deviation and unstable working temperature) may lead to the malfunction of ESP8266EX, resulting in the decrease of overall performance.

1.4.5. RF

The output impedance of RF pin (Pin 2) is 50 ohm. Normally, when the antenna impedance approaches 50 ohm, antenna matching is not necessary. However, some low-price antennas commercially available in the market do not feature 50 ohm impedance. Besides, the impedance in 2.4 G to 2.5 G frequency band is rather scattered. Therefore, N-type matching network is essential in circuit design to facilitate antenna matching.

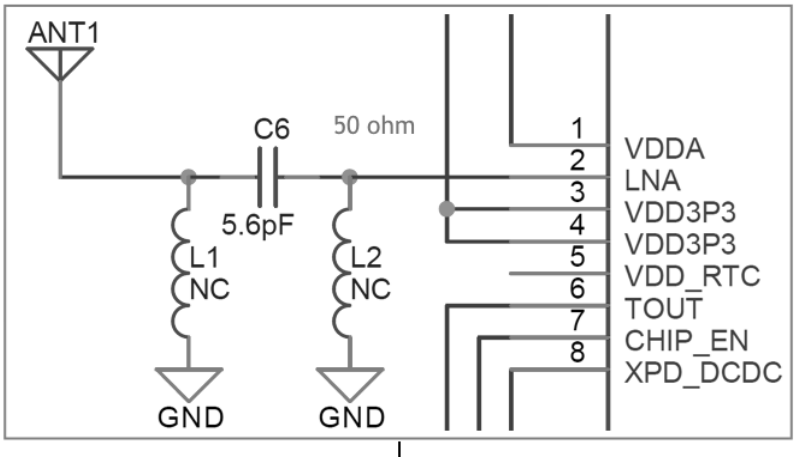


Figure 1-8: ESP8266EX RF

1.4.6. External Resistor 12K

An external ground resistor should be connected o ERS12K pin (Pin31). The ground resistor requires high accuracy when controlling the bias current. An accuracy of 12K±1% is recommended.

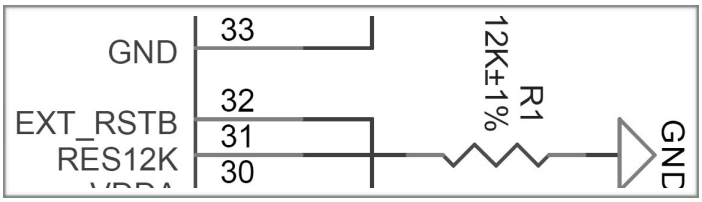


Figure 1-9: ESP8266EX external resistor

1.5. Layout Design

Two layout designs are introduced in this section:

- Standalone ESP8266EX module
- ESP8266EX module as salve device

1.5.1. Standalone ESP8266EX Module

Layout Design

The printed circuit board has four layers:

- The first layer is the TOP layer for signal lines and components
- The second layer is the GND layer, no signal lines are laid so as to ensure an entire plain GND plane.
- The third layer is the POWER layer where only power lines can be placed. It is acceptable to place some signal lines under unavoidable circumstances.
- The forth lay is the BOTTOM layer. Only signal lines can be laid. It is not recommended to place components on this layer.

Power Supply Design

3.3 V power lines are highlighted in Figure 1-10. The total width of the power line should be larger than 15 mil.

Before the power line reaches the analog power-supply pins (including Pin 1, 3, 4, 28, 29) of ESP8266EX, a 10 uF 0603 or 0603 capacitor (C6 in Figure 10) needs to be added. The capacitor should be placed adjacent to the analog power-supply pins of the chipset.

Power lines should be placed on the third layer. When the power lines reached the pins of the chipset, VIAs are needed so that the power lines can go through the layers to connect the pins of the chipset on the TOP layer. The diameter of the VIA holes should exceed the width of power lines and the drilling should be a little bit larger than the radius of VIA.

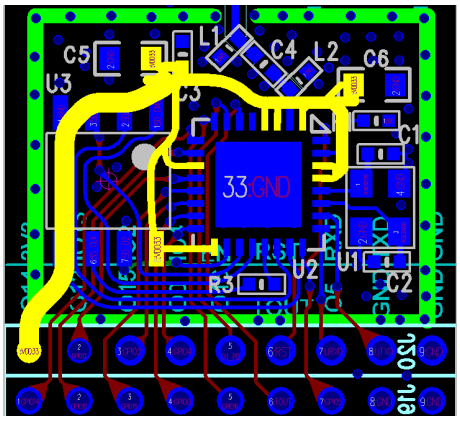


Figure 1-10: ESP8266EX PCB layout

Crystal Oscillator Design

Crystal oscillator should be placed adjacent to the XTAL Pins, the connection lines should not be too long, and need to be wrapped up for shelter.

The input and output lines cannot be punched, crossed or cross the layer.

The input and output bypass capacitor should be located at the left or right side of the chipset; Do not place it on the lines.

No high frequency digital signal lines shall be placed under the four layers of the crystal oscillators. The ideal scenario is that no signal lines is placed under the crystal oscillator. The TOP layer for crystal oscillator should be as large as possible.

No magnetic components such as high current inductance should be placed near to crystal oscillator.

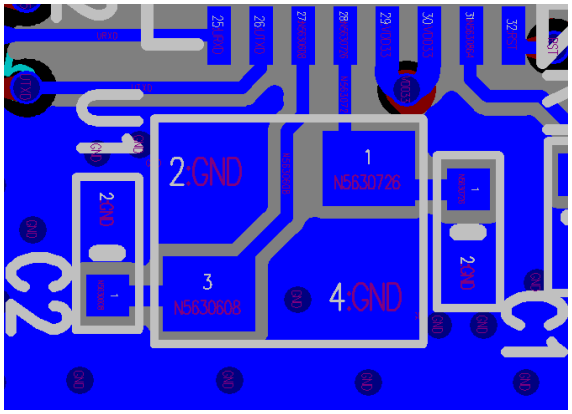


Figure 1-11: ESP8266EX crystal oscillators

RF Design

The characteristic impedance that RF lines control is 50 Ω, in order to ensure the complete board on the second layer. The surrounding drilled hole should be blocked and the lines should be as short as possible. The width of RF lines should be not less than 6 mil, and above 10 mil is better.

A π matching circuit near the RF Pin should be reserved in RF lines. RF lines connecting the chip and antenna should not cover drills, which means cross layer lines are not allowed.

RF lines should not be set at a vertical, or a 45-degree angle. Circular lines are allowed if necessary. No signal lines of high frequency should be set near RF lines.

RF antenna should be set away from high frequency transmitting devices, such as crystal oscillators, DDR, and certain high frequency clocks (SDIO_CLK, etc).

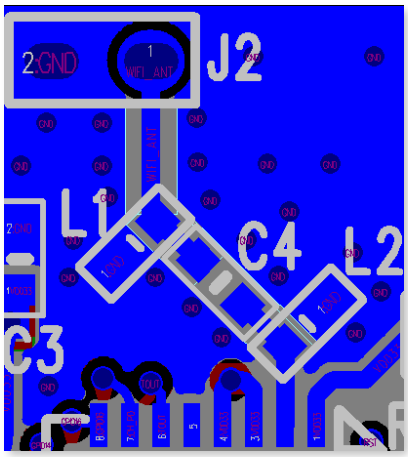
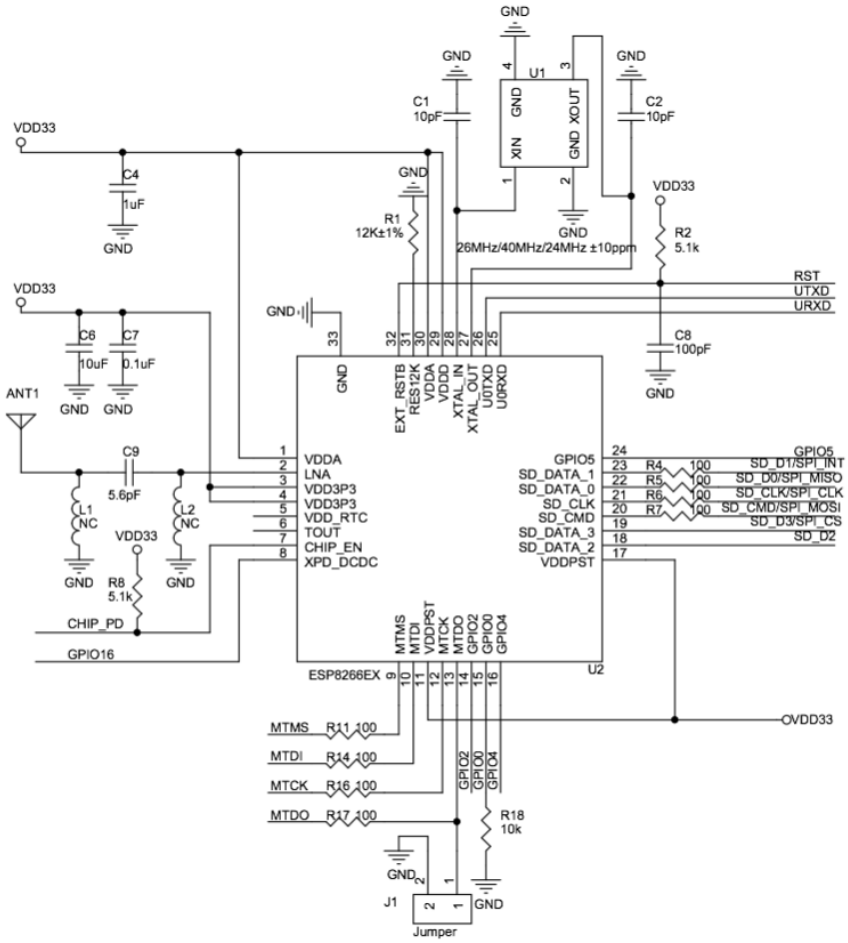


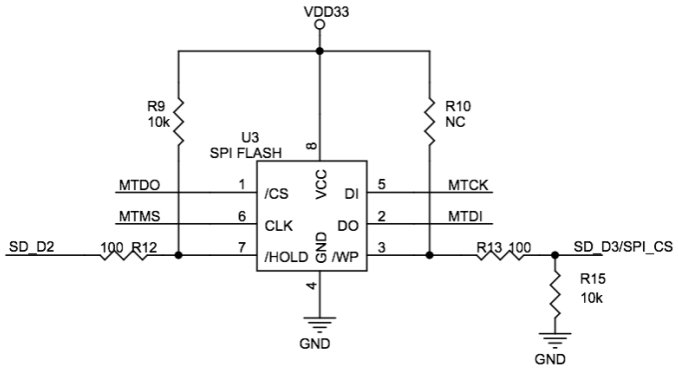
Figure 1-12: ESP8266EX RF

1.5.2. ESP8266EX as Slave Device

When ESP8266EX works with other master CPU as a slave device, signal integrity in layout design is more important than the standalone mode. It is important to keep ESP8266EX away from the interferences caused by complicity of the system and high frequency signals.



1. UART DOWNLOAD MODE: short this jumper
2. SDIO BOOT MODE: disconnect this jumper



1. Quad (recommend) /Dual SPI flash
2. 8Mbit (recommend)
3. sop-150mill

Figure 1-13: Schematic of ESP8266EX as a slave device

Notes:

1. CHIP_PD, as an enable pin, should be connected to a GPIO of Host CPU.
2. Dual SPI Flash (DIO/DOUT): Remove R12, R13, R15 and keep R10, R9.
3. Quad SPI Flash (QIO/QOUT): Remove R9, R10 and keep R13, R12, R15.
   a. 1 bit SDIO: No need to connect SD_D2 and SD_D3 to Host.
   b. SPI: SD_D3 is reused as SPI_CS and no need to be connected to Host.

Take the mainboard of PAD or TV BOX as an example, following aspects shall be noted in system design.

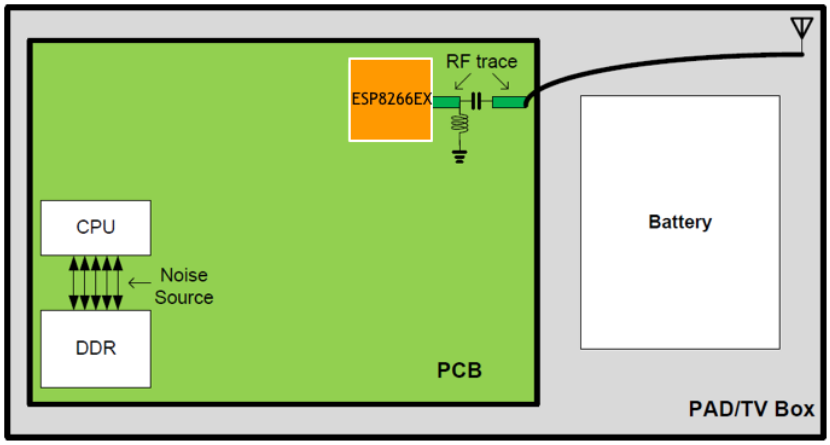


Figure 1-14: PCB plane layout

As shown in Figure 1-14, ESP8266EX is on the edge of PCB and away from CPU and DDR which are the noise source interfering with Wi-Fi frequency in the air. The distance between chipset and CPU + DDR decrease the interference and reduces the coupling noise.

It is suggested to add a 200 Ω series resistor to the six signal lines when ESP8266EX communicates with CPU via SDIO to decrease the drive current and interference, and also eliminate the sequence problem caused by the inconsistent length of SDIO lines.

PCB on-board antenna is not recommended as it receives larger interference and coupling noise which impact RF performance. It is suggested to use external antenna which is directed away from PCB board via cable and weaken the high frequency interference to Wi-Fi.

The high frequency signal lines between CPU and MEM should be noted. The line layout should comply with the high frequency signal regulations (refer to the relative documents about DDR lines layout). CLK and data/addr lines should be lined underground.

The GND of Wi-Fi circuit and other high power devices should be separated and connected through wires if there are electric machines in system design.

Antenna should keep away from noise source of high frequency, such as LCD, HDMI, Camera Sensor, USB, etc.

1.5.3. Typical Layout problems and solutions

Q: The current ripple is not large, but the TX performance of RF is rather poor.

Analysis:

Ripple has a strong impact on the performance of RF TX. It should be noted that ripple must be tested when ESP8266EX sends normal packets. The ripple increases when the power gets high. Generally, the ripple should be <80 mV when sending 11N MCS7 packets; the ripple should be <120 mV when sending 11B packets.

Solution:

Add a10 uF filter capacitor to the branch of source circuit (ESP8266EX AVDD pin). The 10 uF capacitor should be adjacent to the VDDA pin.

Q: The power ripple is small and the TX performance of the chip is poor.

Analysis:

Besides power supply ripple, poor RF TX performance could also be due to the choice of a wrong crystal. For example, the crystal has low quality-factor or the crystal frequency offset is too big — when the frequency offset is more than ±40 ppm, ESP8266EX will not work properly and the performance degrades. Sometimes, the crystal could also be corrupted by other interfering signals, such as output digital signals or input signals. Another possible issue is the coupling from inductors or antenna to the crystal. Usually the crystal can filter such interferers but a large enough amplitude may affect performance.

Solution:

This problem is caused by improper layout and can be solved by re-layout. See Chapter 1.5 for details.

Q: When ESP8266EX is sending data packages, the power value tested by an instrument is much higher or lower than the target power value, and the EVM is relatively poor.

Analysis:

The difference between the power value tested by an instrument and the target power value can be caused by the impedance mismatch of the chipset RF pin to the antenna.

Solution:

Reserve a π type circuit on the RF wiring which allows match of the resistance with the antenna, so the resistance from the chipset RF pin to antenna approaches 39-j6 Ω, which usually gives the best performance.

Q: TX performance is not bad, but the RX sensitivity is low.

Analysis:

Good TX performance means proper RF impedance matching. External coupling to the antenna can influence the RX performance. For instance, the crystal oscillator signal's harmonics could couple to the antenna. If ESP8266EX serves as slave device, there will be other high frequency interferers or high speed digital signal interference sources on the board.

Solution:

Keep the antenna away from crystal oscillators and keep RF trace lines away from high frequency signals.

1.6. Application

1.6.1. Wi-Fi Smart Hardware Converted from UART Serial Ports

The two UART interfaces are defined as Table 1-3.

Table 1-3: Pin definitions of UART interfaces

Category	Pin definition	Function
UART0	(Pin 25) U0RXD+ (Pin 26) U0TXD	Receive and transmit user's data packages
UART1	(Pin 14) GPIO2 (U1TXD)	Print information

AT+ instructions relevant documentations are provided with software.

Application example: ESP8266EX development board (see Chapter 2).

1.6.2. Sensor

ESP8266EX can be used in sensor products, using the I2C interface. The I2C works in the master mode and can connect to multiple sensors. The slave devices is identified through addressing mode (each slave device has a unique address identity).

The sensor products send the real-time data to ESP8266EX via I2C interface, and ESP8266EX uploads the data to server wirelessly. Users can acquire information from server through applications when the mobile phone connects to internet.

1.6.3. Smart Light

ESP8266EX can be used to develop smart home products, such as smart light using PWM and infrared interfaces. Three PWM interfaces controls red, blue, and green LEDs respectively. The minimal PWM duty ratio is $1/2^{14}$. In addition, infrared interfaces allows specific control on LEDs, such as rest, power on/off, color switch, etc.

1.6.4. Smart Plug

ESP8266EX can be used for developing smart plug products. The GPIOs control the power switch through the high/low levels switch and connection/disconnection of relay. Such an application comprises of three modules: 220 V to 3.3 V power conversion module, ESP8266EX Wi-Fi module and relay control module.

2. ESP-LAUNCHER

2.1. Overview

Espressif provides ESP8266EX development board - ESP Launcher for quick configuration and further development. The size of the board is 46 mm x 78.5 mm (see Figure 2-1).

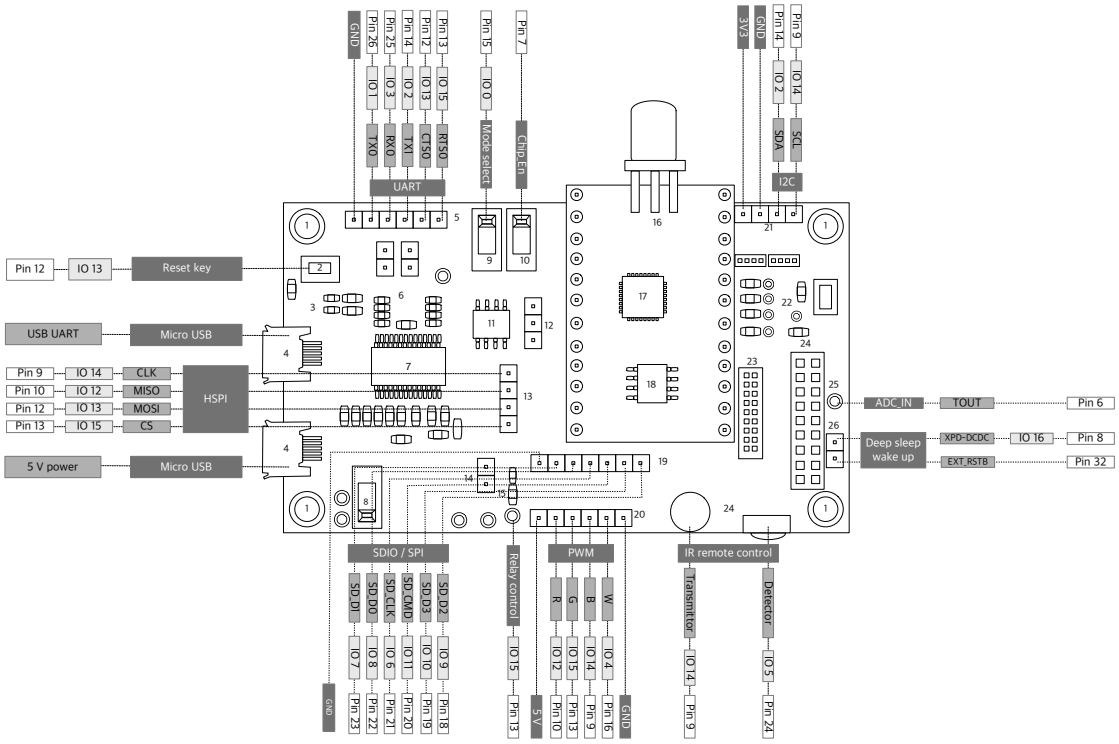


Figure 2-1: ESP-LAUNCHER

1	Location hole	8	5 V power switch	15	Relay control	22	Undefined LEDs and keys
2	Reset key	9	IO0 control	16	SMA ANT	23	1.27 mm double pitch
3	Wi-Fi LED, Link LED	10	CH_EN switch	17	Test board	24	2.0 mm double pitch
4	Micro USB: USB-UART, 5 V power	11	Flash2: HSPI	18	Flash1: SPI	25	ADC_IN
5	UART	12	CS of Flash2	19	SDIO/SPI	26	Deep sleep wake up
6	UART SWAP	13	HSPI	20	IR_T, IR_R		
7	USB-UART chip	14	3.3 V power	21	I2C		

ESP-LAUNCHER can be configured through USB serial connection or Wi-Fi. The module functionalities are described in Table 2-1.

Table 2-1: ESP-LAUNCHER module description

Module	Functional description

MICRO USB interface	Two USB interfaces. Both can be used for 5 V power supply or serial communication (Figure 2-1-4).
Power supply	USB interface provides 5 V power supply which can be converted to 3.3 V through DC/CD converter. One light indicating the power, and a skip stitch for testing the power current.
Slide switch	Three slide switches are used for 5 V power supply (Figure 2-1-8), GPIO0 voltage level switch (Figure 2-1-9) and chip enable pin CH_EN (Figure 2-1-10). When a switch is pulled up, the voltage level is high. When a switch is pulled down, the voltage level is low. Pull up the power switch to power on the board, and pull down the switch to power off the board. Pull up the GPIO0 switch to enter Flash boot mode. UART debug tool can be used to debug. Pull down the GPIO0 switch to enter UART Download mode to download software to Flash through ESP Flash Tool.
Reset Key	SW1 is connected to MTCK (GPIO13) for application reset including reset Wi-Fi configurations (Figure 2-1-2). SW2 is not defined (Figure 2-1-22).
Indicator light	Red light (D2) indicates Wi-Fi work status (Figure 2-1-3). Blue (D3) indicates communication with server (Figure 2-1-3). Green light (D1) is an indicator light for relay switch control (Figure 2-1-15) Blue light (D11) and red light (D10) indicate Rx and Tx work status (Figure 2-1-7) Red light (D12) indicates 5 V power supply (Figure 2-1-8). D4/13/14/16 are to be defined (Figure 2-1-22).
Jumper	J82: It needs to be short-circuited by a jumper, so 3.3 V power supply can be connected to other circuits. It can also be used to test power current (Figure 2-1-14). J3: Chip select for HSPI flash. HSPI flash is disabled when the upper two pins are short-circuited by a jumper. HSPI flash is enabled when the bottom two pins are shorted circuited by jumper (Figure 2-1-12). J14 and J67: Short circuit J14 to connect GPIO13 to U0CTS. Short circuit J67 to connect GPIO15 to U0RTS (Figure 2-1-6). J77: Short circuit J77 to connect GPIO16 to EXT_RSTB to awake the device from deep sleep (Figure 2-1-26).
Interfaces	UART, HSPI, SDIO/SPI, I2C, ADC_IN, GPIO16, relay control, PWM and IR TX/RX
Flash	Flash1 (the one mounted on the test board): Flash1 is connected to the chipset using SPI interface. Currently, Flash1 is mainly used when the chip is working under WiFi standalone mode. R9 and R85 can be used as chip select of Flash1. By default, Flash 1 is enabled (Figure 2-1-18). Flash2 (the one mounted on the baseboard): Flash2 is connected to the chipset using HSPI interface. HSPI is mainly used in SIP mode, in this application, ESP8266EX chipset is used as slave device, and is connected to the host MCU using the SPI interface that is defined in standard SDIO interface. HSPI is connected to Flash2. J3 can be used as chip select of Flash2 (Figure 2-1-11).
Testing modules	There are several modules that can be connected with ESP-LAUNCHER development board for testing and development, including the test board that is mounted on the baseboard, modules with1.27mm double-row needles (Figure 2-1-23), and 2.00mm double-row needles. It should be noted that pins of the modules should be connected with corresponding pins on the baseboard. Besides, only one type of module can be used at one time.

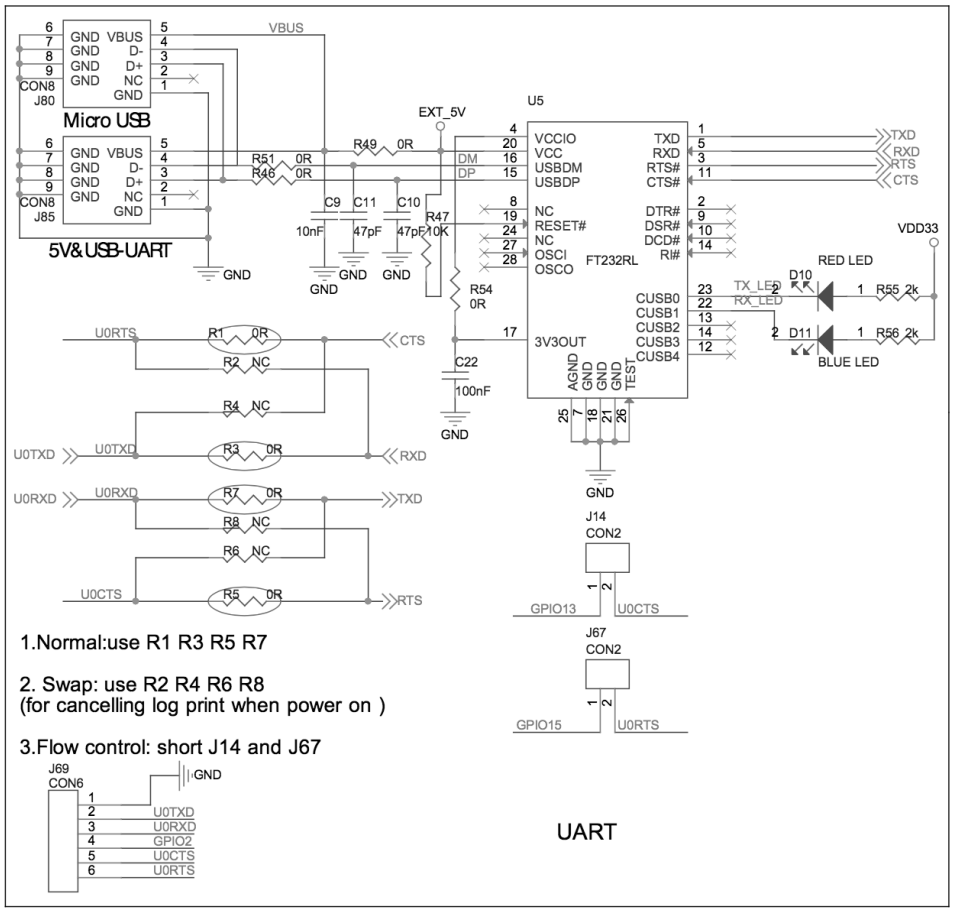
The interfaces on ESP-LAUNCHER are described in Table 2-2.

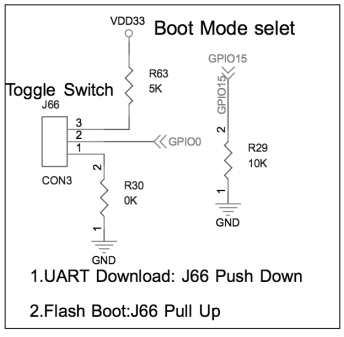
Table 2-2: ESP-LAUNCHER interfaces

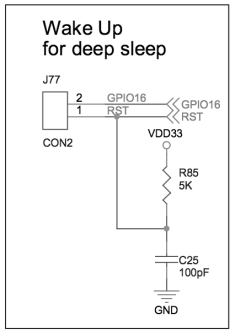
Interfaces	Function description
HSPI	SPI Flash 2, display screen, and MCU can be connected using HSPI interface (Figure 2-1-13).
SDIO/SPI	Flash, host MCU, display screen, etc. can be connected using SDIO/SPI interface (Figure 2-1-19).
PWM	Currently the PWM interface has four channels, users can extend the channels as needed. PWM interface can be used to control LED lights, buzzers, relays, electronic machines and etc (Figure 2-1-20).
IR	The functionality of infrared remote control interface can be implemented via software programming. NEC coding, modulation and demodulation are used by this interface. The frequency of modulated carrier signal is 38KHz (Figure 2-1-24).
ADC	ESP8266EX is embedded with a 10-bit precision SARADC. ADC_IN interface is used to test the power supply voltage of VDD3P3 (Pin 3 and Pin 4), as well as the input voltage of TOUT (Pin 6). It can be used in sensors (Figure 2-1-25).
I2C	Sensors and display screens with 2.54mm and 1.27mm needles can be connected using I2C interface (Figure 2-1-21).
UART	UART0 : U0TXD , U0RXD , MTDO (U0RTS) , MTCK (U0CTS) UART1 : GPIO2 (U1TXD) Device with UART interfaces can be connected (Figure 2-1-5).
	Downloading: U0TXD+U0RXD or GPIO2+U0RXD Communicating: UART0: U0TXD, U0RXD, MTDO(U0RTS), MTCK(U0CTS) Debugging: UART1_TXD (GPIO2) can be used to print debugging information.
	By default, UART0 will output some printed information when the device is powered on and is booting up. If this issue exerts influence on some specific applications, users can exchange the inner pins of UART when initializing, that is, exchange U0TXD, U0RXD with U0RTS, U0CTS. R1/3/5/7 should not be mounted with other components, while R2/4/6/8 can be mounted with other components. J14 and J67 should be short-circuiting connected.
Relay control terminal	Relay control terminal is used to control the switch on-and-off of smart plugs with an indicator light (Figure 2-1-15).

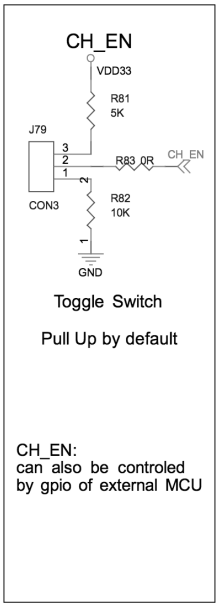
2.2. Schematics

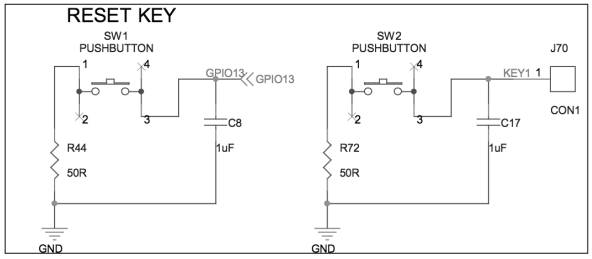
2.2.1. Interfaces











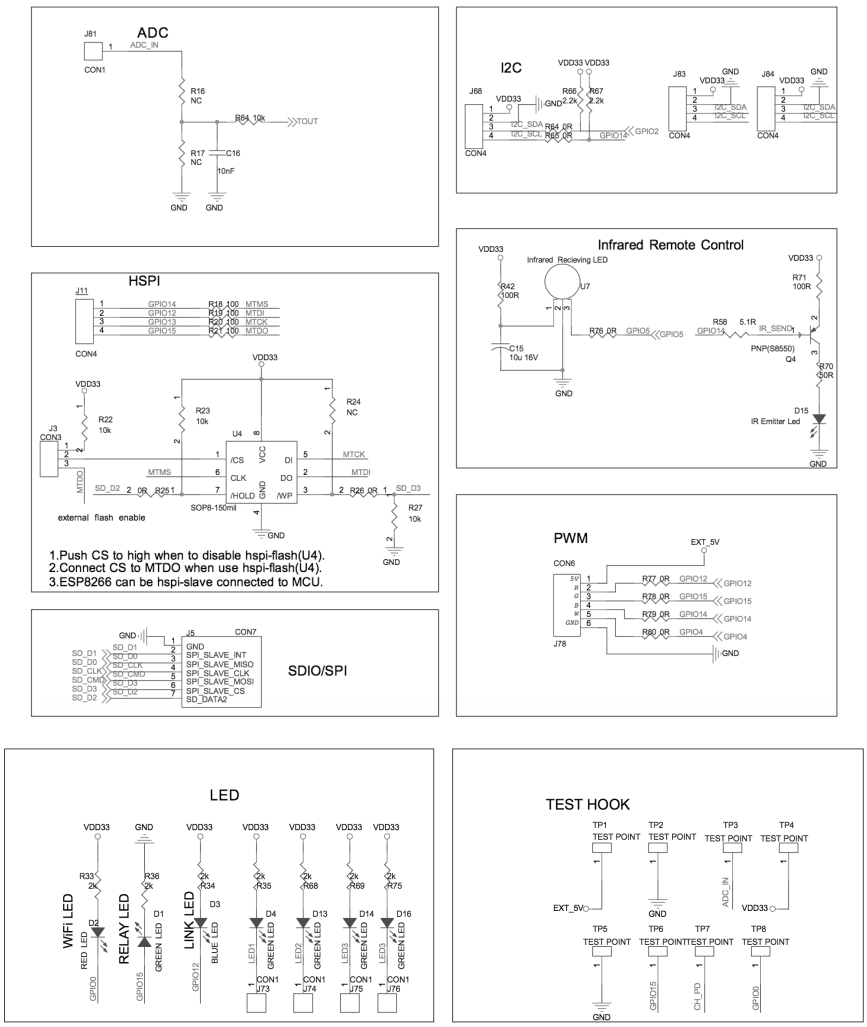


Figure 2-2: ESP-LAUNCHER interface schematics

2.2.2. 5V Power Supply

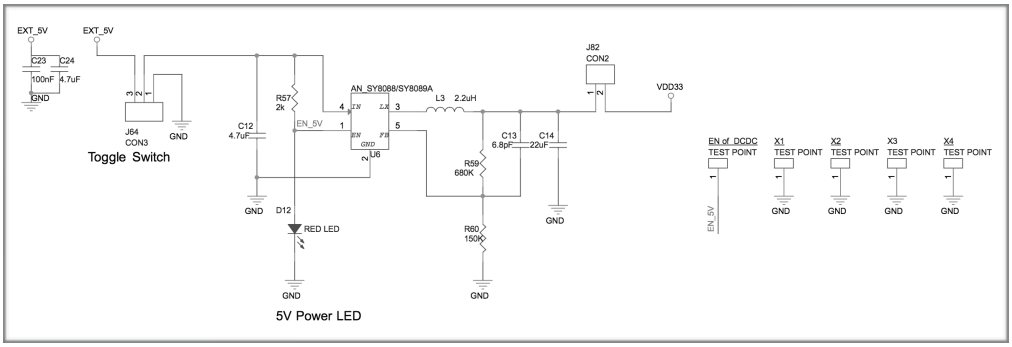


Figure 2-3: ESP-LAUNCHER 5V power supply schematics

2.2.3. Test Module

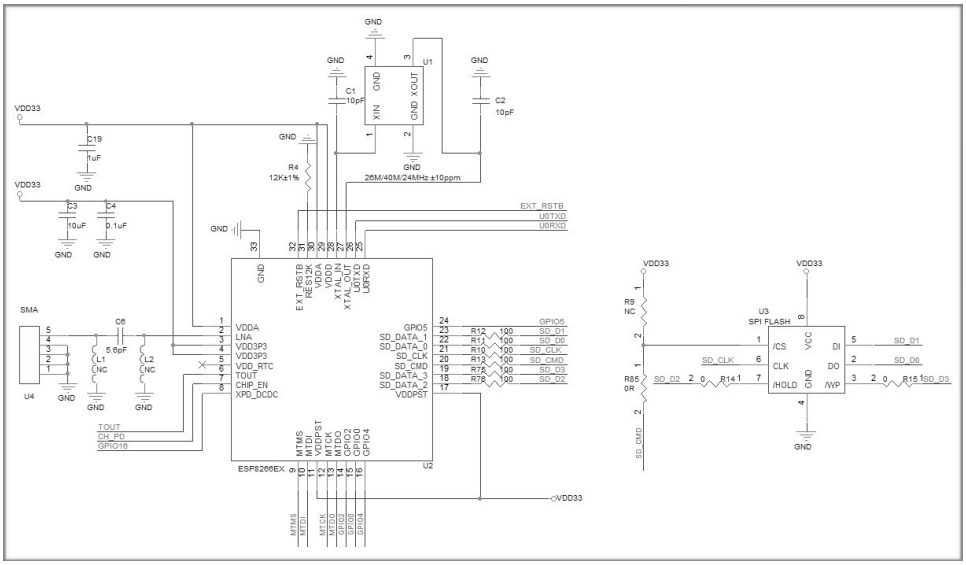


Figure 2-4: ESP-LAUNCHER test module schematics

2.3. Test Board

A test board is embedded on ESP-LAUNCHER as shown in Figure 2-5. The external size of the test board is 20 mm x 31 mm. An 2DBi SMA antenna or other testing equipment can be connected with the test board via the SMA antenna connector. The spacing of inserting needles on the test board is 2.54 mm, which can be easily inserted into breadboard for testing.

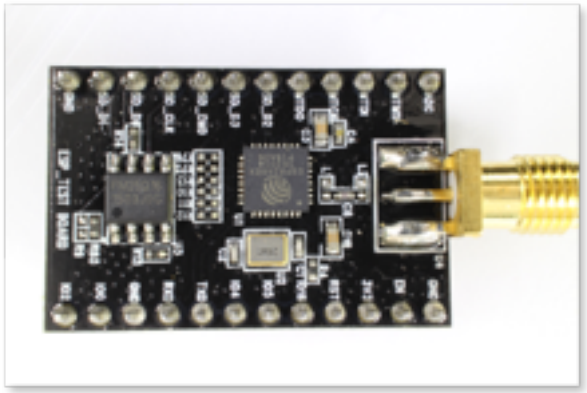


Figure 2-5: ESP-LAUNCHER test board

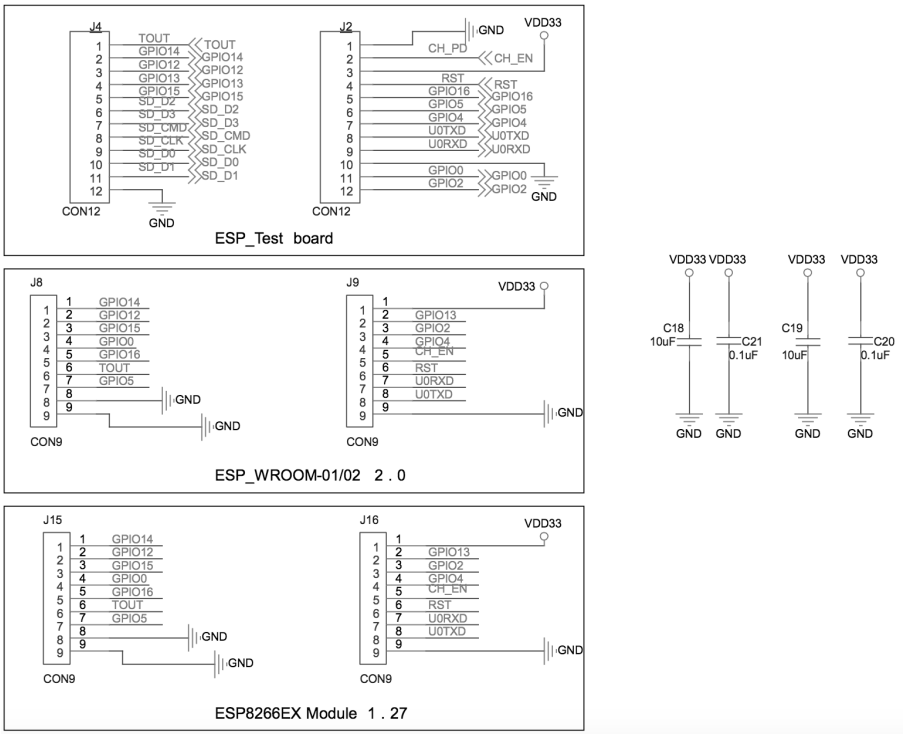


Figure 2-6: ESP-LAUNCHER test board schematics

3. ESP-WROOM

Espressif provides two types of modules, SMD module (ESP-WROOM-02) and DIP module (ESP-WROOM-01). It is recommended to use these modules for test or further development with ESP8266EX chipset.

3.1. SMD Module ESP-WROOM-02

The pin distribution of the SMD Module is illustrated in Figure 16. The external size of the module is 18 x 20mm. The type of flash used on this module is an SPI flash with package size SOP8-150mil. The antenna applied on this module is a 3DBi PCB-on-board antenna.

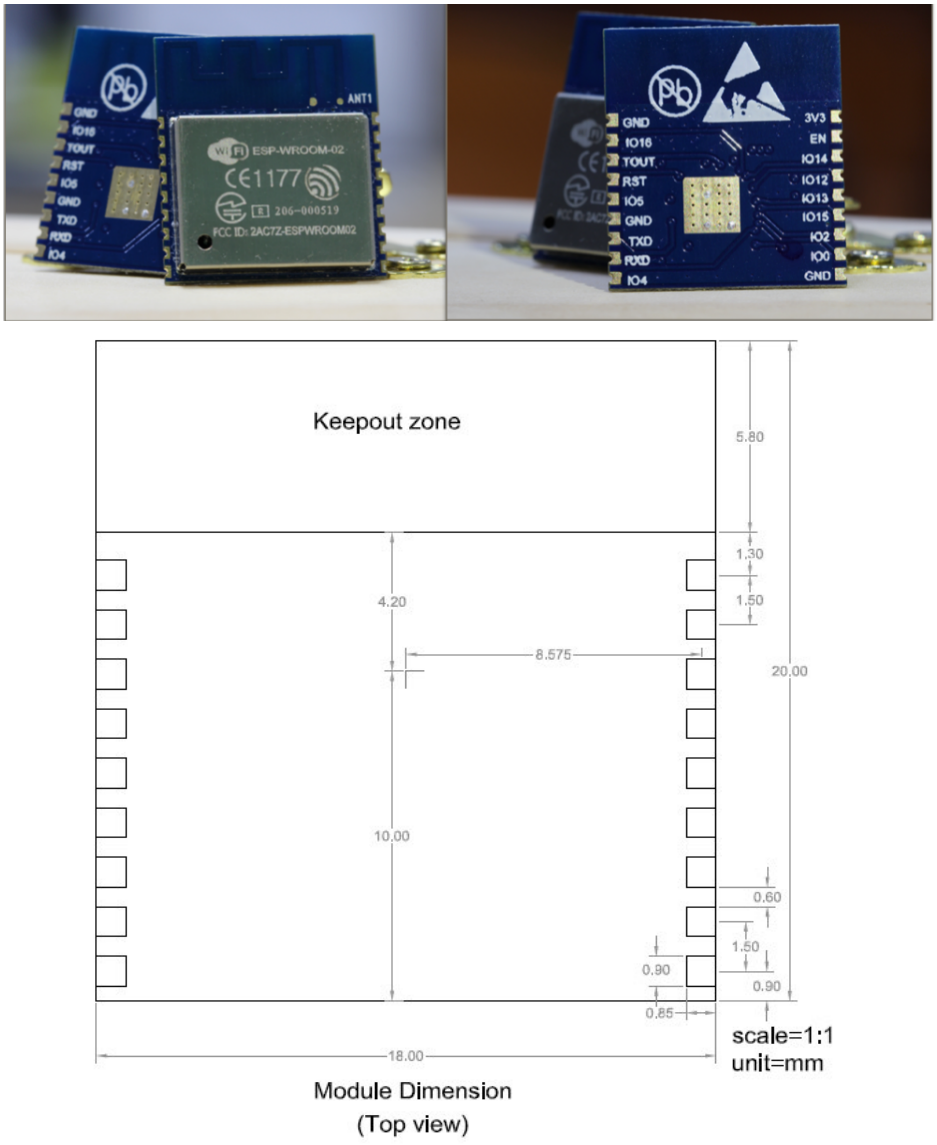


Figure 3-1: Dimensions of ESP-WROOM-02

There are altogether 18 pinouts. The pin distribution and definitions are listed in Table 3-1 below:

Table 3-1: ESP-WROOM-02 pinout

NO.	Pin name	Function
1	3V3	3.3V power supply (VDD)
2	EN	Chip enable pin. Active high
3	IO14	GPIO14; HSPI_CLK
4	IO12	GPIO12; HSPI_MISO
5	IO13	GPIO13; HSPI_MOSI; UART0_CTS
6	IO15	GPIO15; MTDO; HSPICS; UART0_RTS
7	IO2	GPIO2; UART1_TXD
8	IO0	GPIO0
9	GND	GND
10	IO4	GPIO4
11	RXD	UART0_RXD; GPIO3
12	TXD	UART0_TXD; GPIO1
13	GND	GND
14	IO5	GPIO5
15	RST	Reset
16	TOUT	It can be used to test the power-supply voltage of VDD3P3 (Pin3 and Pin4) and the input power voltage of TOUT (Pin 6). These two functions cannot be used simultaneously.
17	IO16	GPIO16; Wake up the chipset from deep sleep mode when connected to RST pin.
18	GND	GND

Notes :

1. Connect the 3.3V power-supply pin to an external 3.3V power source, for 3.3V is the power-supply for both analog circuit and digital circuit.
2. EN pin is Wi-Fi enable pin. Set EN pin high for normal working.
3. SMD Module features two working modes: UART Download mode and Flash Boot mode. In UART Download mode, programs can be written into the Flash or Memory by flash tool. If the programs are burnt into the Memory, the programs can run only when the device is powered on. Once the device is powered off, the programs in the Memory will be erased. However, when the programs are burnt into the Flash, they will be stored and can be invoked and used at any time.
4. Before the module is powered on, pin GND RXD TXD should be lead out and be connected with USB to TTL serial cable (FT232 is suggested) to download, print log and communicate.
5. The whole operating process can be examined through the log information printed by UART interface. If the programs written into the Flash do not function in the right way, check the initial settings of the working mode through logs printed from a serial port.
6. Serial printing tools (for example, SecureCRT) and flash tool cannot open the serial port simultaneously.

By default the Flash is empty. Follow the procedures below to download the programs into the Flash.

1. Pull IO15 and IO0 to low-voltage level, leave IO2 dangled to set the module to work under UART Download mode.
2. Download the programs into Flash with ESP Flash Tool (Refer to “ESP Flash Tool User Manual”).
3. After downloading the programs into Flash, pull down IO15 to low-voltage level, keep IO2 dangled, and pull up IO0 to high-voltage level. The module is then shifted from UART Download mode to the Flash Boot mode.
4. Power on the chip, the programs will be read and executed during the initialization.

——END

3.2. DIP Module ESP-WROOM-01

The size of the DIP module is 18 x 19 mm. The Flash type applied is a SPI flash packed in SOP8-150mil. The antenna used is a 1 DBi metal antenna. The 2.00mm double pitch applied can be both vertical or straight, depending on specific applications. Refer to Table 6 for pin definitions of this module.

Figure 3-2: ESP-WROOM-01

⚠Notice :

The DIP metal antenna is thin and prone to distortion. Change the antenna immediately if the shape and appearance are abnormal.

3.3. Schematics

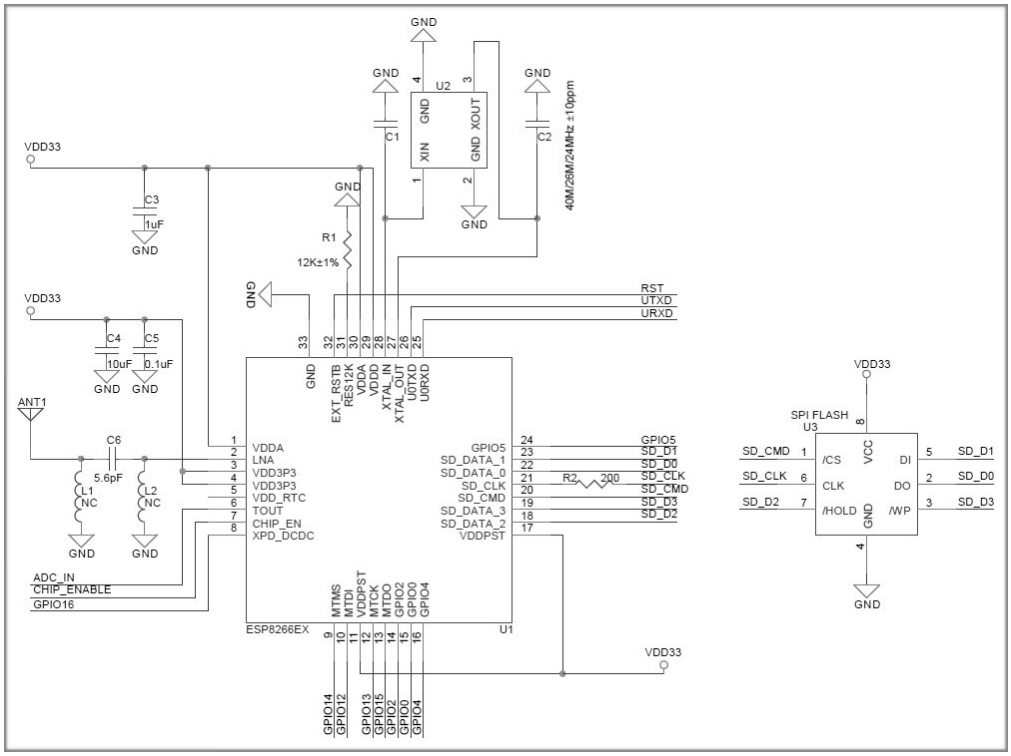


Figure 3-3: ESP-WROOM schematics

Espressif IOT Team

http://bbs.espressif.com