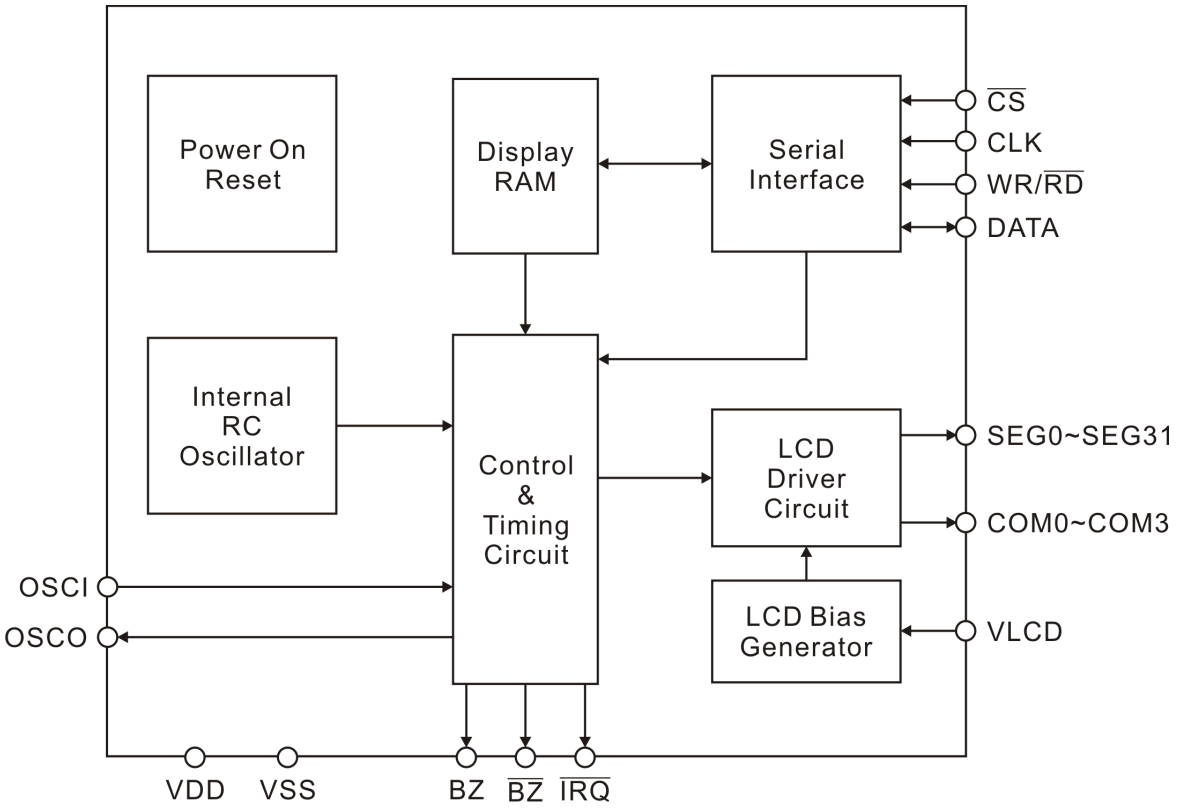
DESCRIPTION

The PT1621 is a RAM mapping, 128 dots (32x4) and multi-function LCD driver. The host can program PT1621 easily by three or four lines interface. Many S/W configuration features make PT1621 suitable for multiple LCD applications. PT1621 also includes S/W power down command to reduce power consumption.

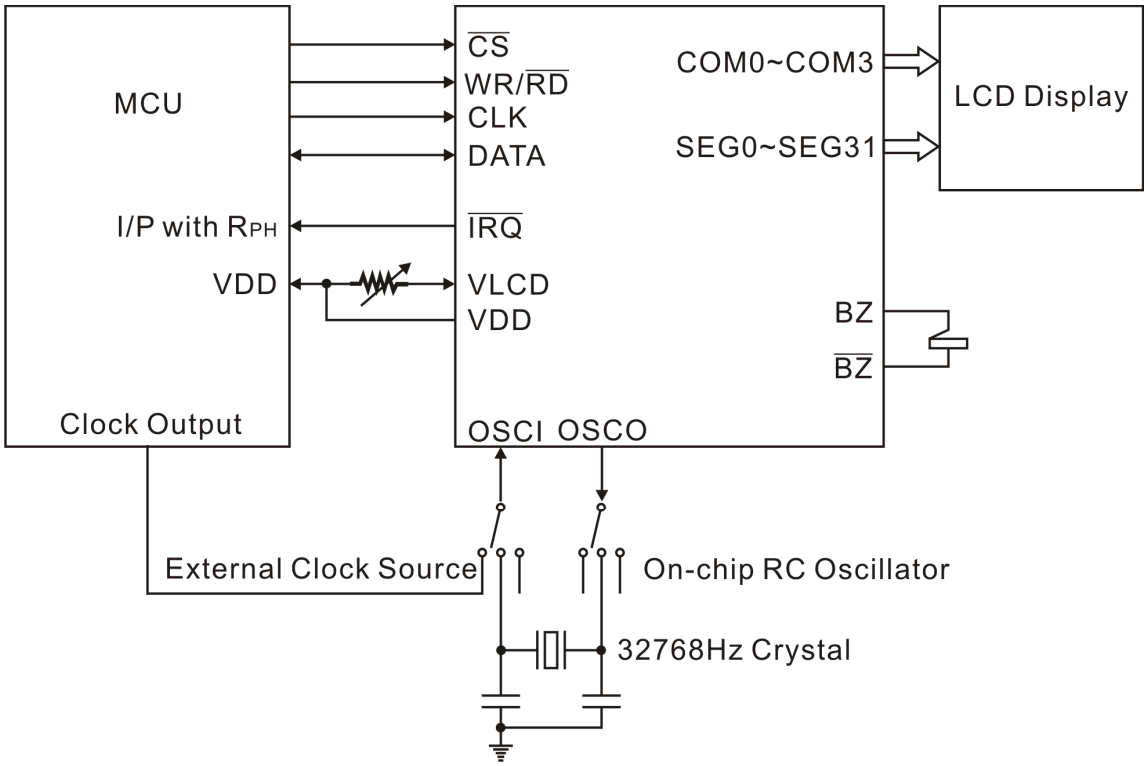
FEATURES

- Operating voltage: 2.2V~5.5V
- LCD operating voltage can be adjusted by VLCD pin
- Built-in 256KHz RC oscillator
- External 32.768KHz crystal or 256KHz frequency source input
- Two selectable tone (buzzer) frequencies (2KHz/4KHz)
- Built-in time base generator and WDT
- Time base or WDT overflow output
- 8 kinds clock sources of time base/WDT
- Internal LCD driving frequency source
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- 32 x 4 LCD driver
- Built-in POR circuit
- Built-in 32 x 4 bit display RAM
- 3 or 4-wire serial interface
- Power down command reduces power consumption
- Software configuration feature
- Data mode and command mode instructions
- R/W address auto increment
- Three data accessing modes
- Package type:
  - PT1621-LQ: 44pin LQFP
  - PT1621-X: 48pin SSOP
  - PT1621-G: Gold bumped chip

BLOCK DIAGRAM



APPLICATION CIRCUIT

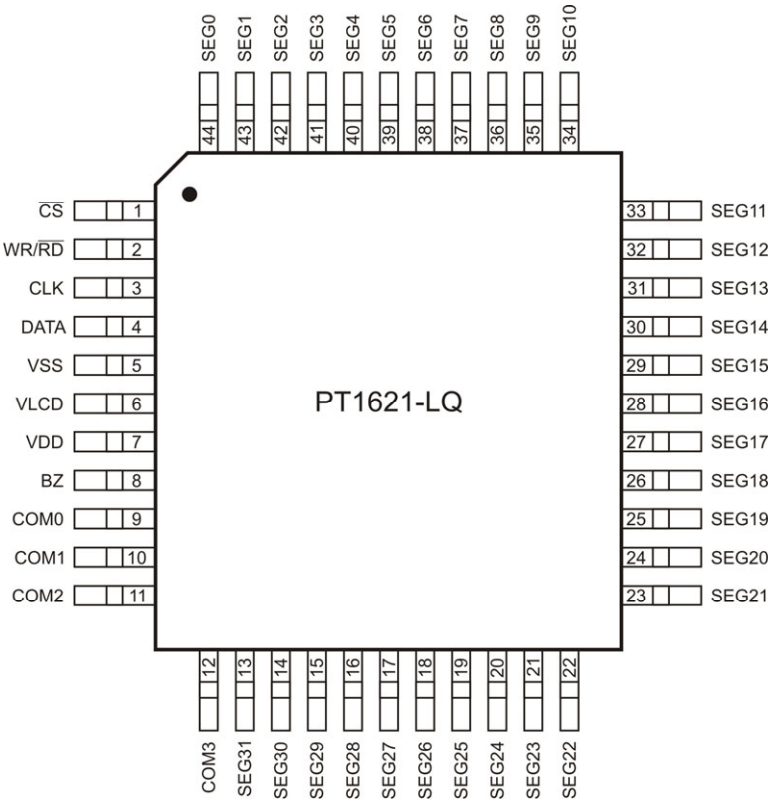


ORDER INFORMATION

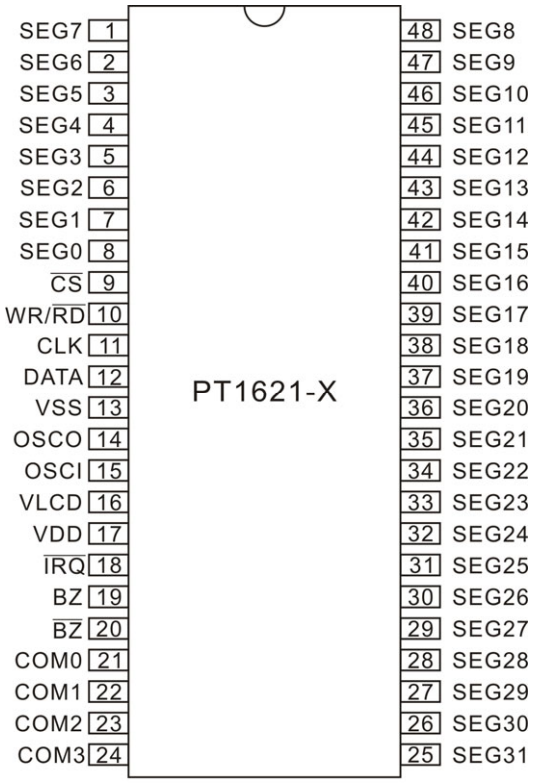
Valid Part Number	Package Type	Top Code
PT1621-LQ	44 Pins, LQFP	PT1621-LQ
PT1621-X	48 Pins, SSOP, 300MIL	PT1621-X
PT1621-G	COG	-

PIN CONFIGURATION

44 PINS, LQFP



48 PINS, SSOP



PIN DESCRIPTION

Pin Name	I/O	Function	Pin No.	
			44pin LQFP	48pin SSOP
SEG7~SEG0	O	LCD segment outputs	37~44	1~8
$\overline{CS}$	I	Chip selection input with pull-high resistor. When the $\overline{CS}$ is logic high, the data and command read/write are disabled. The communication be enabled only $\overline{CS}$ is logic low.	1	9
WR/$\overline{RD}$	I	Write and read control with internal pull-high resistor	2	10
CLK	I	Data and command write/read clock input with internal pull-high resistor.	3	11
DATA	I/O	Serial data input/output with internal pull-high resistor.	4	12
VSS	-	IC negative power supply, ground.	5	13
OSCO	O	32.768KHz crystal oscillator for system clock. When clock set as external clock, the external clock source should be connected to the OSCI pin. The OSCI and OSCO pins can be opened when the internal RC OSC is selected.	-	14
OSCI	I		-	15
VLCD	-	LCD power supply.	6	16
VDD	-	IC positive power supply.	7	17
$\overline{IRQ}$	O	Time base or WDT overflow interrupt output. (NMOS open drain output)	-	18
BZ	O	Buzzer outputs (2KHz or 4KHz)	8	19
$\overline{BZ}$	O	Buzzer outputs (2KHz or 4KHz)	-	20
COM0~COM3	O	LCD common outputs	9~12	21~24
SEG31~SEG8	O	LCD segment outputs	13~36	25~48

FUNCTION DESCRIPTION

DISPLAY MEMORY (DISPLAY RAM)

The display RAM includes 32x4 bits and mapped to the contents of the LCD driver directly. The data in the display RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands from HOST. The LCD display will not be interfered when HOST executes READ, WRITE or READ-MODIFY-WRITE commands. The following is the RAM mapping to LCD pattern.

	COM3	COM2	COM1	COM0	
SEG0					0
SEG1					1
SEG2					2
SEG3					3
:		:			:
SEG31					31
	D3	D2	D1	D0	Addr / Data

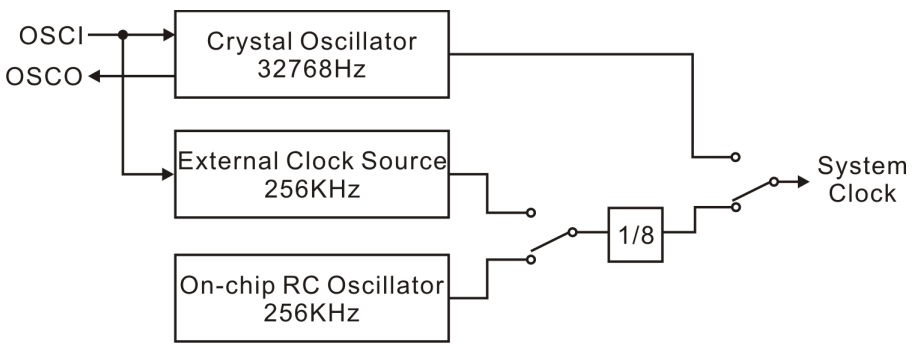
Address 6 bits
(A5, A4, …, A0)

Data 4 bits
(D3, D2, D1, D0)

RAM Mapping

SYSTEM OSCILLATOR

There are three kinds of clock source can be selected by S/W setting, an internal 256KHZ RC OSC, an external crystal oscillator 32.768KHz or an external 256KHz. After the SYS DIS command is executed, the system clock will be stopped and the LCD bias generator will be turned off. The SYS DIS command is usable only for the on-chip RC oscillator or for the crystal oscillator. When the system clock is stopped, the LCD display will become blank and function of time base/WDT will be stopped. The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. It should be noticed, when using external clock source as the system clock, the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32KHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256KHz clock source operation. At the initial system power on, the PT1621 is at the SYS DIS state.



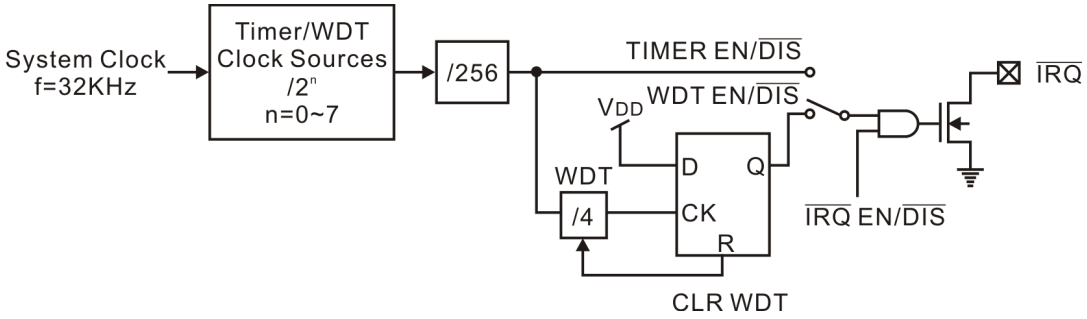
System Oscillator Configuration

TIME BASE AND WATCHDOG TIMER (WDT)

The time base generator is comprised by an 8-stage count-up counter. The watch dog timer (WDT) is comprised of an 8-stage time base generator along with a 2-stage counter-up counter. The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the $\overline{IRQ}$ output by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation:

$f_{WDT}=32KHz/2^n$, where the value of n ranges from 0 to 7 by command options.

If the 256KHz frequency is chosen (internal or external), the frequency source is pre-scaled to 32KHz firstly. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. The WDT DIS command disables the time base generator, the WDT EN command will enables the time base generator and the WDT time-out flag output. The TMR EN command will disconnect the output of WDT from the IRQ pin, and connect the output of the time base generator to the IRQ pin. The CLR WDT command will clear WDT output. Set CLR WDT or CLR TMR command will clear the value of the time base. The CLR WDT or the CLR TMR command should be executed firstly to the WDT EN or the TMR EN command respectively. Before executing the IRQ EN command the CLR WDT or CLR TMR command should be executed first. When changing the mode from WDT to time base, the CLR TMR command should be executed firstly. Once the WDT time-out occurs, the IRQ pin will stay at a logic low level until the CLR WDT or the IRQ DIS command is issued. IRQ is an open drain output, IRQ DIS command keeps IRQ output as floating status. The IRQ EN makes the output of the time base generator or of the WDT time-out flag appear on the IRQ pin. The IRQ output can be enabled or disabled by executing the IRQ EN or the IRQ DIS command, respectively. The configurations of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by S/W commands. At the power down mode the time base/WDT loses all its functions. The IRQ is disabled after the system power on.



Timer and WDT Configuration

TONE OUTPUT (BUZZER OUTPUT)

PT1621 built-in tone generator. BZ and $\overline{BZ}$ are pair of differential driving output used to drive a piezo buzzer. Tone frequency 4KHz or 2KHz can be selected by S/W command. When the system is disabled or the tone output is inhibited, the logic level of BZ and $\overline{BZ}$ will keep low level.

LCD DRIVER

The PT1621 can be configured as 1/2 or 1/3 bias and 1/2, 1/3 or 1/4 duty by S/W configuration. This function makes the PT1621 suitable for multiple LCD applications. The LCD clock is 256Hz, depend on different duty mode, the scan rate is different. Ex. Scan duty is 1/4 then the scan rate will be 256Hz/4=64Hz. The following are summarized of the LCD corresponding commands.

Name	Command Code	Function
LCD OFF	**100**00000010X	Turn off LCD output and bias
LCD ON	**100**00000011X	Turn on LCD output and bias
BIAS & COM	**100**0010aaXbX	b=0: 1/2 bias b=1: 1/3 bias aa=00: 2 commons aa=01: 3 commons aa=10: 4 commons

The protection diodes of LCD COMMON and SEGMENT outputs are connected to VDD.

COMMAND FORMAT

There are DATA and COMMAND modes from HOST to PT1621. The COMMAND mode ID is “1 0 0”, The COMMAND consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode includes READ, WRITE and READ-MODIFY-WRITE operations.
The following are the data mode IDs and the command mode ID:

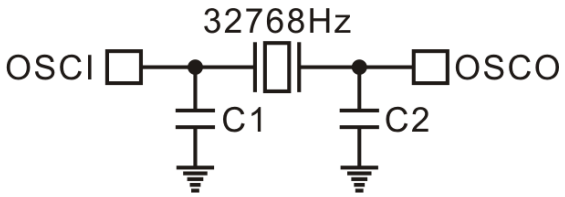
Operation	Mode	ID
Read	Data	110
Write	Data	101
Read-modify-write	Data	101
Command	Command	100

INTERFACING

The host and PT1621 using 4 lines as communicated interface. We suggest host can not use open drain output to drive these 4 communicated interface. $\overline{CS}$, CLK, WR/$\overline{RD}$ and DATA. Access will not be executed when $\overline{CS}$ is high. DATA pin is a bi-direction pin and transmit the data to read or write. The WR/$\overline{RD}$ line is used to control the direction of data transferring between the host controller and PT1621. Data in the RAM are clocked out on the falling edge of the WR/$\overline{RD}$ and rising edge of CLK signals. The clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data at least 300ns (t_{DS3}) delayed after falling edge of the WR/$\overline{RD}$ (D_0) or rising edge of CLK (D_1~D_3) signals. The data, address, and command on the DATA line are all clocked into the PT1621 on the rising edge of the CLK signal when WR/$\overline{RD}$ = "1". The $\overline{IRQ}$ pin can be selected as a WDT overflow flag output or timer output by the S/W setting.

CRYSTAL SELECTION

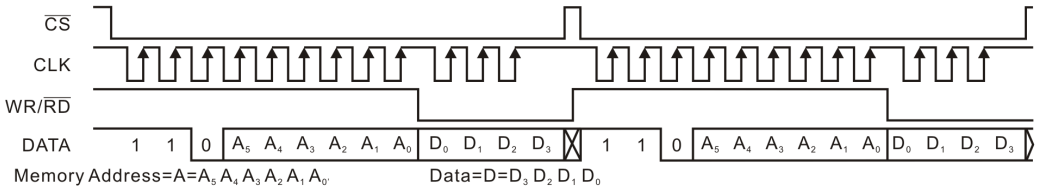
PT1621 can connect a 32768Hz crystal directly via OSCI and OSCO. Two external capacitors C1 and C2 are needed for corrective frequency. The following table is suggested value of C1 and C2. The start time of Oscillator will be affected by different value of C1 and C2. It should be noticed when user change the value of C1 and C2.



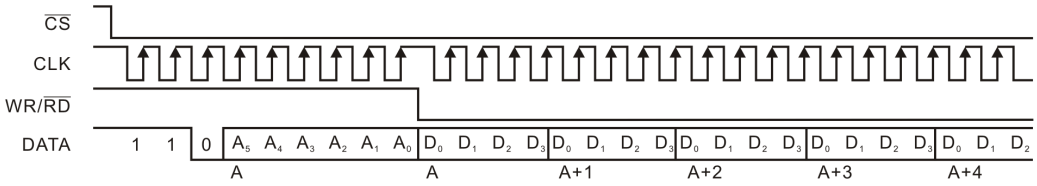
Crystal Error	Capacitor Value
±25ppm	0~4pF
±25~46ppm	4~10pF
±46~63ppm	10~20pF

SERIAL INTERFACE TIMING DIAGRAMS

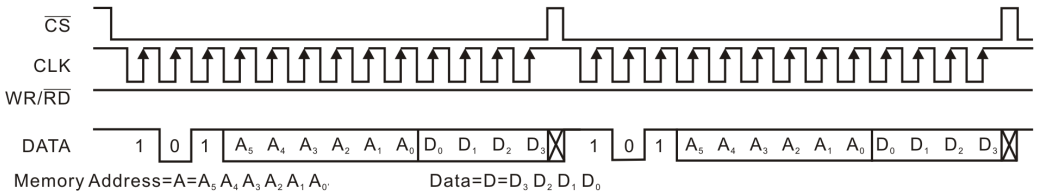
Read mode (Command code “110”) ↑↓ : write latch input and read latch output



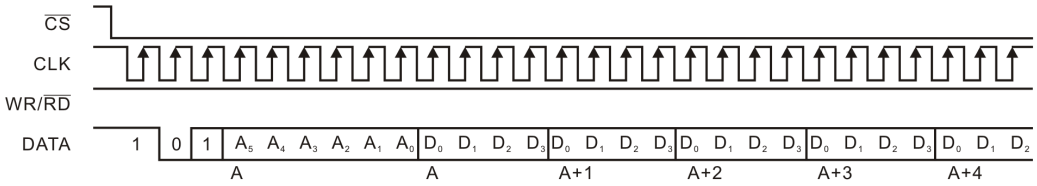
Read mode (Successive address reading)



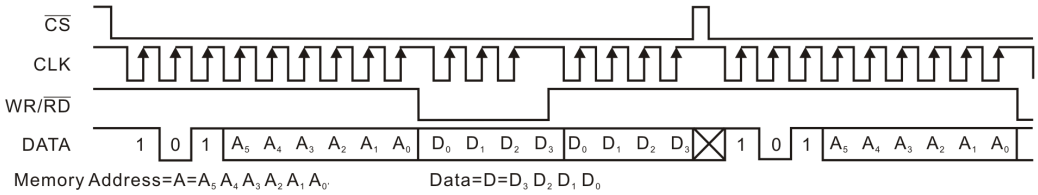
Write mode (Command code “101”)



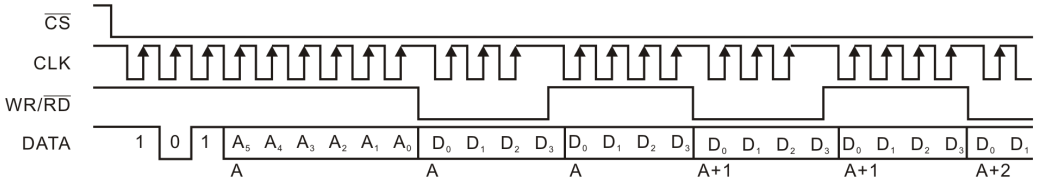
Write mode (Successive address writing)



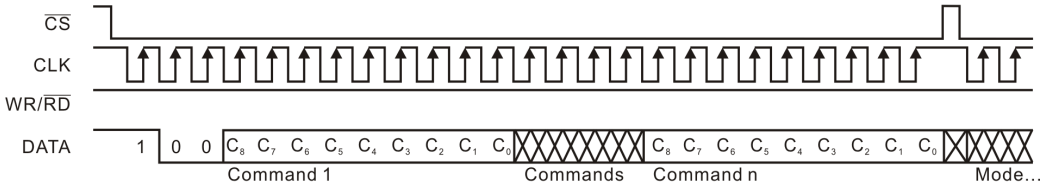
Read-modify-write mode (Command code “101”)



Read-modify-write mode (Successive address accessing)



Command mode (Command code “100”)



COMMAND SUMMARY

Name	ID	Command code	D/C	Function	Reset
READ	110	$A_5A_4A_3A_2A_1A_0D_0D_1D_2D_3$	D	Read data from RAM	-
WRITE	101	$A_5A_4A_3A_2A_1A_0D_0D_1D_2D_3$	D	Write data to RAM	-
READ-MODIFY-WRITE	101	$A_5A_4A_3A_2A_1A_0D_0D_1D_2D_3$	D	Read/write data from/to RAM	-
DISSYS	100	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
ENSYS	100	0000-0001-X	C	Turn on system oscillator	-
LCDOFF	100	0000-0010-X	C	Turn off LCD bias generator	Yes
LCDON	100	0000-0011-X	C	Turn on LCD bias generator	-
DISTMR	100	0000-0100-X	C	Disable time base output	-
DISWDT	100	0000-0101-X	C	Disable WDT time-out flag output	Yes
ENTMR	100	0000-0110-X	C	Enable time base output	-
ENWDT	100	0000-0111-X	C	Enable WDT time-out flag output	-
BZOFF	100	0000-1000-X	C	Turn off tone (buzzer) outputs	Yes
BZON	100	0000-1001-X	C	Turn on tone (buzzer) outputs	-
CLRTMR	100	0000-11XX-X	C	Clear the contents of time base generator	-
CLRWDT	100	0000-111X-X	C	Clear the contents of WDT stage	-
XT32K	100	0001-01XX-X	C	System clock source=crystal oscillator	-
RC256K	100	0001-10XX-X	C	System clock source=on-chip RC oscillator	Yes
EXT256K	100	0001-11XX-X	C	System clock source=external clock source	-
BIASD2	100	0010-aaX0-X	C	LCD 1/2 bias option aa=00: 2 commons option aa=01: 3 commons option aa=10: 4 commons option	-
BIASD3	100	0010-aaX1-X	C	LCD 1/3 bias option aa=00: 2 commons option aa=01: 3 commons option aa=10: 4 commons option	-
BZ4K	100	010X-XXXX-X	C	Tone (buzzer) frequency=4KHz	Yes
BZ2K	100	011X-XXXX-X	C	Tone (buzzer) frequency=2KHz	-
DISIRQ	100	100X-0XXX-X	C	Disable IRQ output	Yes
ENIRQ	100	100X-1XXX-X	C	Enable IRQ output	-
F1	100	101X-X000-X	C	Time base/WDT clock output: 1Hz The WDT time-out flag after: 4s	-
F2	100	101X-X001-X	C	Time base/WDT clock output: 2Hz The WDT time-out flag after: 2s	-
F4	100	101X-X010-X	C	Time base/WDT clock output: 4Hz The WDT time-out flag after: 1s	-
F8	100	101X-X011-X	C	Time base/WDT clock output: 8Hz The WDT time-out flag after: 1/2s	-
F16	100	101X-X100-X	C	Time base/WDT clock output: 16Hz The WDT time-out flag after: 1/4s	-
F32	100	101X-X101-X	C	Time base/WDT clock output: 32Hz The WDT time-out flag after: 1/8s	-
F64	100	101X-X110-X	C	Time base/WDT clock output: 64Hz The WDT time-out flag after: 1/16s	-
F128	100	101X-X111-X	C	Time base/WDT clock output: 128Hz The WDT time-out flag after: 1/32s	Yes
TEST	100	1110-0000-X	C	Test mode, user don't use.	-
NORMAL	100	1110-0011-X	C	Normal mode	Yes

Notes:
1. X: don't care
2. COM and SEG stay at "1" when LCDOFF and DISSYS
3. DISSYS=DISSYS + LCDOFF, Restart from DISSYS ➔ ENSYS and LCDON
4. DISSYS or LCDOFF ➔ The outputs of COM and SEG stay at VLCD
5. CLRWDT=CLRWDT + CLRTMR
6. F1 ~ F128=set timer time-base frequency and WDT overflow time output to IRQ (if ENIRQ)
7. Timer time-out=time-base frequency output to IRQ (if ENIRQ)
8. WDT time-out=time-out output latched to IRQ (if ENIRQ)
9. DISIRQ only disable the IRQ output, WDT latched data is not affected
10. BIAS setting and common options are independent
11. If a COM is disabled, the output waveform will be de-selected duty waveform

ABSOLUTE MAXIMUM RATINGS

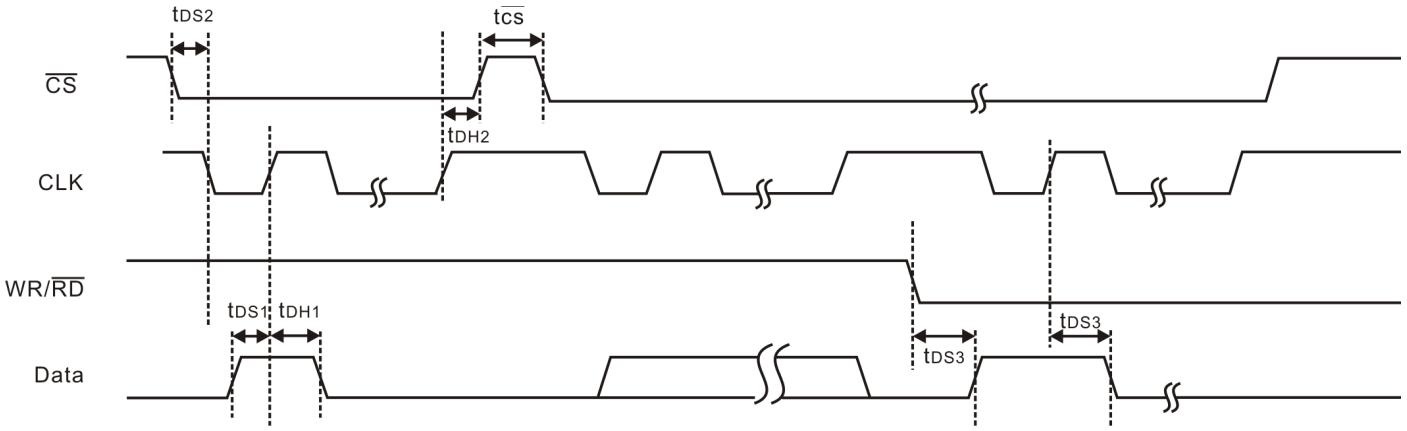
Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	VSS_0.3V to VSS+5.5V	V
Input voltage	V_I	VSS_0.3V to VDD+0.3V	V
Operating temperature	Topr	-40~85	℃
Storage temperature	Ststg	-50~125	℃

DC CHARACTERISTICS

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating voltage	-	-	2.2	-	5.5	V
I_{DD1}	Operating current	5	On-chip RC oscillator, No load and LCD on	-	300	600	μA
I_{DD2}	Operating current	5	Crystal oscillator, No load and LCD on	-	120	240	μA
I_{DD3}	Operating current	5	External clock source, No load and LCD on	-	200	400	μA
I_{STB}	Standby current	5	Power down and no load	-	0.2	2	μA
V_{IH}	Input high voltage	5	DATA, $\overline{CS}$, WR/$\overline{RD}$, CLK	4.0	-	5.0	V
V_{IL}	Input low voltage	5	DATA, $\overline{CS}$, WR/$\overline{RD}$, CLK	0	-	0.8	V
I_{OH1}	DATA, BZ, $\overline{BZ}$	5	V_{OH}=0.9V_{DD}	-0.9	-1.8	-	mA
I_{OL1}	DATA, BZ, $\overline{BZ}$, $\overline{IRQ}$	5	V_{OL}=0.1V_{DD}	1.3	2.6	-	mA
I_{OH2}	LCD COM source current	5	V_{OH}=0.9V_{LCD}, V_{LCD}=V_{DD}	-120	-200	-	μA
I_{OL2}	LCD COM sink current	5	V_{OL}=0.1V_{LCD}, V_{LCD}=V_{DD}	150	250	-	μA
I_{OH3}	LCD SEG source current	5	V_{OH}=0.9V_{LCD}, V_{LCD}=V_{DD}	-70	-100	-	μA
I_{OL3}	LCD SEG sink current	5	V_{OL}=0.1V_{LCD}, V_{LCD}=V_{DD}	120	200	-	μA
R_{PH}	Pull-high resistance	5	DATA, $\overline{CS}$, WR/$\overline{RD}$, CLK	30	60	100	KΩ
V_{LCD}	LCD power supply	-	-	2	-	V_{DD}	V

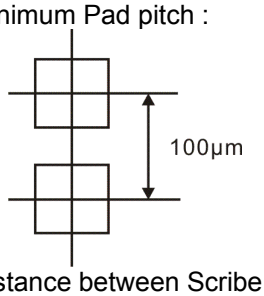
AC CHARACTERISTICS

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System clock	3	On-chip RC oscillator	192	256	320	KHz
f_{SYS2}	System clock	-	External clock	-	256	-	KHz
f_{SYS3}	System clock	-	Crystal oscillator	-	32.768	-	KHz
f_{LCD}	LCD clock	-	On-chip RC oscillator	-	f_{SYS1}/1024	-	KHz
		-	External clock	-	f_{SYS2}/1024	-	KHz
			Crystal oscillator	-	f_{SYS3}/128	-	KHz
t_{COM}	LCD common period	-	n: LCD COM number	-	n/f_{LCD}	-	ms
f_{CLK}	Serial clock frequency	-	Duty=50%	4	-	300	KHz
f_{BZ}	Buzzer output frequency (On-chip RC oscillator)	3	2KHz	1.5	2	2.5	KHz
			4KHz	3	4	5	KHz
$t_{\overline{CS}}$	Chip de-select time	-	Minimum $\overline{CS}$ high time	-	100	250	ns
t_{RST}	Reset to chip enable	-	-	-	-	1	ms
t_{DS1}	DATA write setup time	-	Before write clock	60	120	-	ns
t_{DH1}	DATA write hold time	-	After write clock	250	300	-	ns
t_{DS2}	$\overline{CS}$ setup time	-	Before write/read clock	500	600	-	ns
t_{DH2}	$\overline{CS}$ Hold time	-	After write/read clock	50	100	-	ns
t_{DS3}	DATA read stable time	-	After read clock	250	300	-	ns

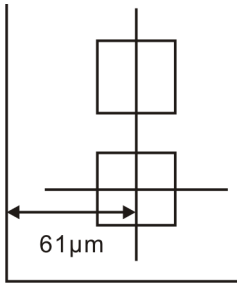


PAD ASSIGNMENT

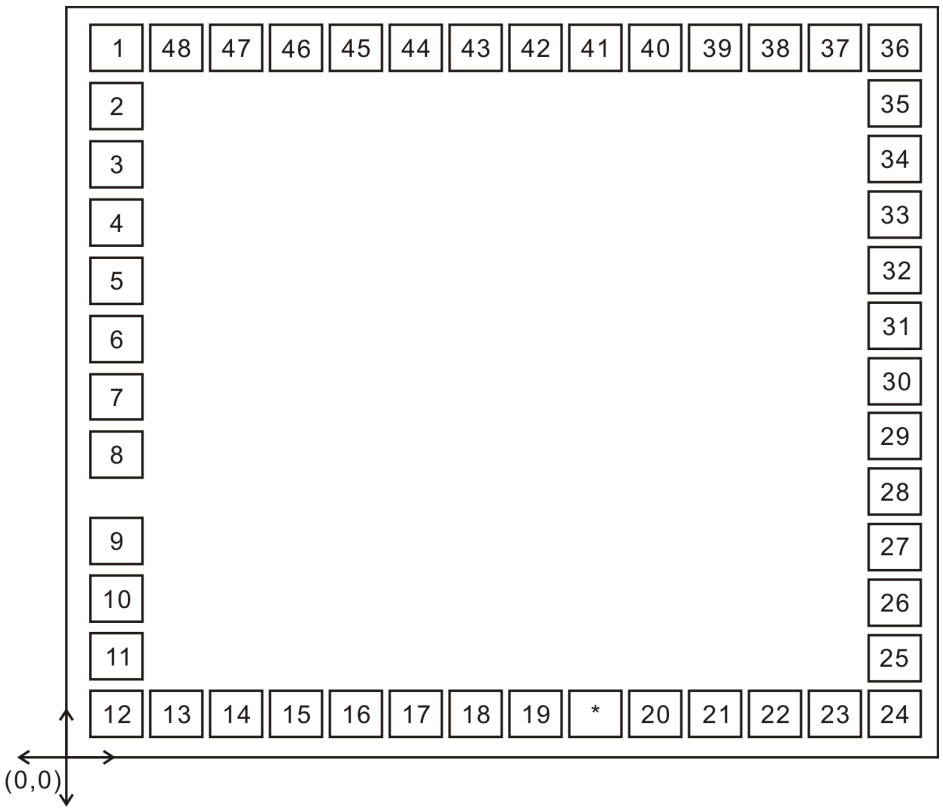
1. Chip size :
2. X=1430μm ± 5μm
   Y=1330μm ± 5μm
3. Pad window size: 85μm x 85μm
4. Wafer thickness: 300μm ± 10μm
5. Minimum Pad pitch :



6. Distance between Scribe line and Pad:



Note: Pad * is SEG27B

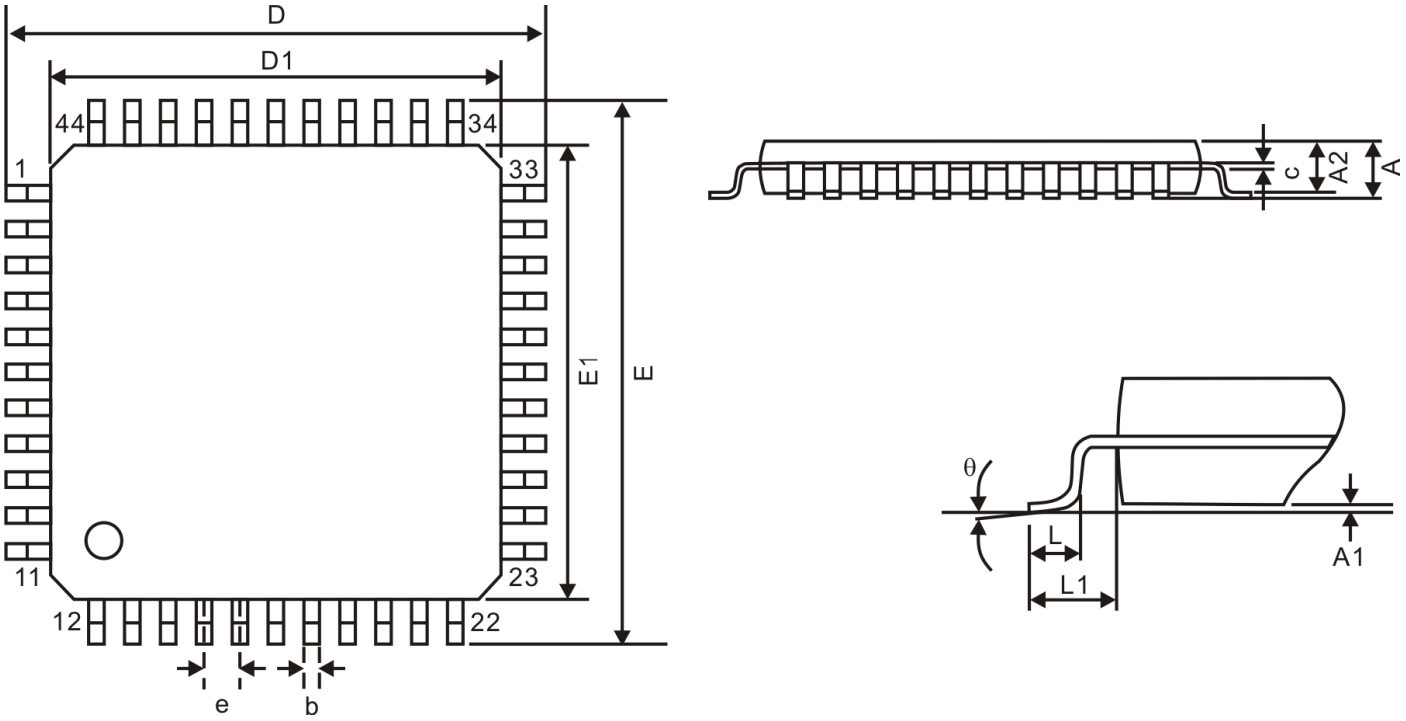


PAD LOCATION

Pad No.	Pad Name	X-axis	Y-axis
1	$\overline{CS}$	47.5	1247.5
2	WR/$\overline{RD}$	47.5	1147.5
3	CLK	47.5	1047.5
4	DATA	47.5	947.5
5	VSS	47.5	838.5
6	OSCO	47.5	729.5
7	OSCI	47.5	620.5
8	VLCD	47.5	511.5
9	VDD	47.5	356.5
10	$\overline{IRQ}$	47.5	247.5
11	BZ	47.5	147.5
12	$\overline{BZ}$	47.5	47.5
13	COM[0]	147.5	47.5
14	COM[1]	247.5	47.5
15	COM[2]	347.5	47.5
16	COM[3]	447.5	47.5
17	SEG[31]	547.5	47.5
18	SEG[30]	647.5	47.5
19	SEG[29]	747.5	47.5
	SEG27B	847.5	47.5
20	SEG[28]	947.5	47.5
21	SEG[27]	1047.5	47.5
22	SEG[26]	1147.5	47.5
23	SEG[25]	1247.5	47.5
24	SEG[24]	1347.5	47.5
25	SEG[23]	1347.5	147.5
26	SEG[22]	1347.5	247.5
27	SEG[21]	1347.5	347.5
28	SEG[20]	1347.5	447.5
29	SEG[19]	1347.5	547.5
30	SEG[18]	1347.5	647.5
31	SEG[17]	1347.5	747.5
32	SEG[16]	1347.5	847.5
33	SEG[15]	1347.5	947.5
34	SEG[14]	1347.5	1047.5
35	SEG[13]	1347.5	1147.5
36	SEG[12]	1347.5	1247.5
37	SEG[11]	1247.5	1247.5
38	SEG[10]	1147.5	1247.5
39	SEG[9]	1047.5	1247.5
40	SEG[8]	947.5	1247.5
41	SEG[7]	847.5	1247.5
42	SEG[6]	747.5	1247.5
43	SEG[5]	647.5	1247.5
44	SEG[4]	547.5	1247.5
45	SEG[3]	447.5	1247.5
46	SEG[2]	347.5	1247.5
47	SEG[1]	247.5	1247.5
48	SEG[0]	147.5	1247.5

PACKAGE INFORMATION

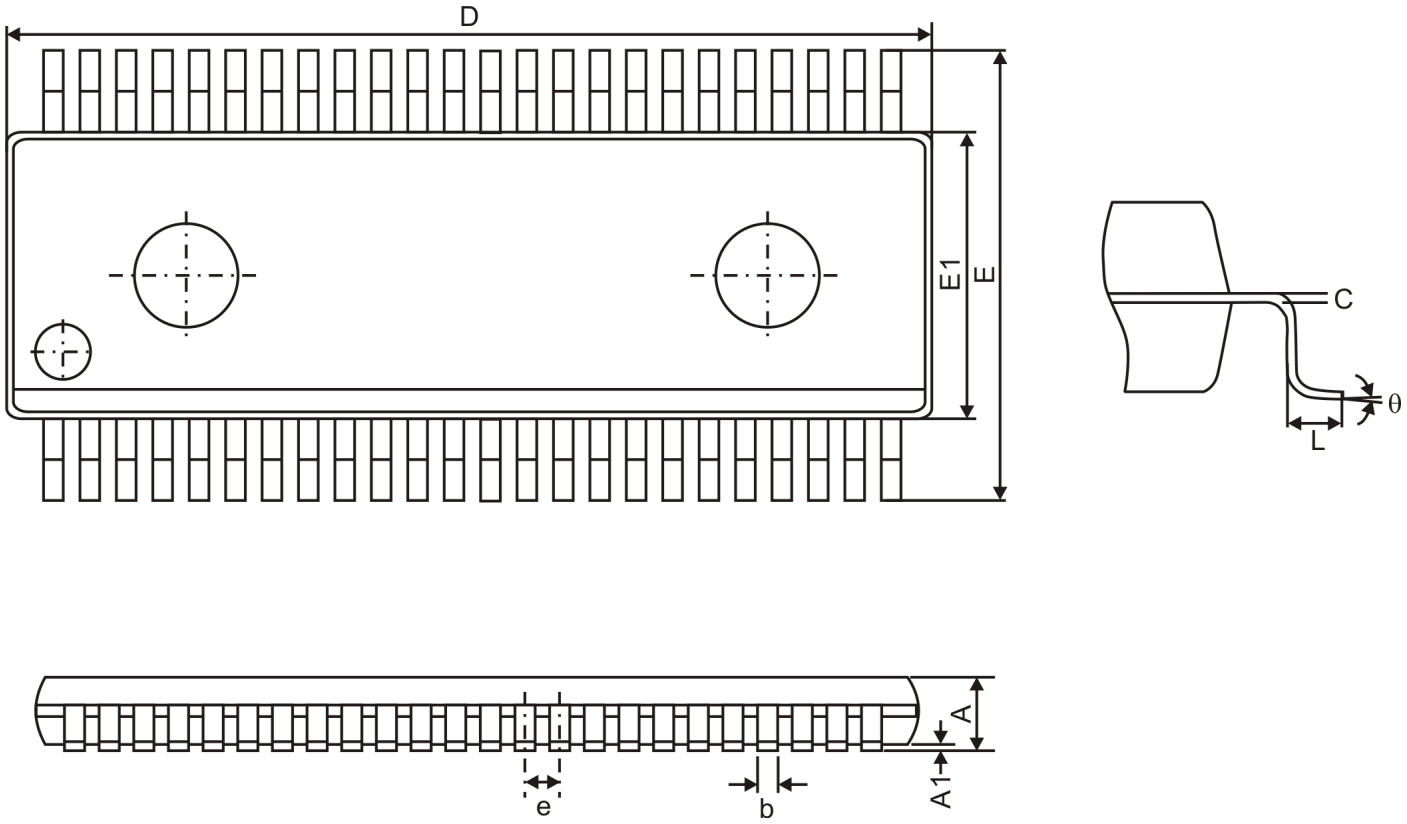
44 PINS, LQFP



Symbol	Dimensions		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	-	0.20
D	12.00 BSC.		
D1	10.00 BSC.		
E	12.00 BSC.		
E1	10.00 BSC.		
e	0.80 BSC		
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

Notes:
1. Refer to JEDEC MS-026.
2. All dimensions are in millimeter

48 PINS, SSOP, 300MIL



Symbol	Dimensions		
	Min.	Nom.	Max.
A	2.41	2.59	2.79
A1	0.20	0.31	0.41
b	0.00	0.25	0.30
C	0.13	-	0.25
D	15.75	15.88	16.00
E	10.03	-	10.67
E1	7.39	7.49	7.60
e		0.64	
L	0.51	-	1.02
θ	0°	-	8°

Notes:
1. Refer to JEDEC MO-118
2. All dimensions are in millimeter

IMPORTANT NOTICE

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