Laurel Electronics Co., Ltd.

LCD Module Specification

Model No.: LC2021-BMDWH6-D

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RECORD OF REVISION

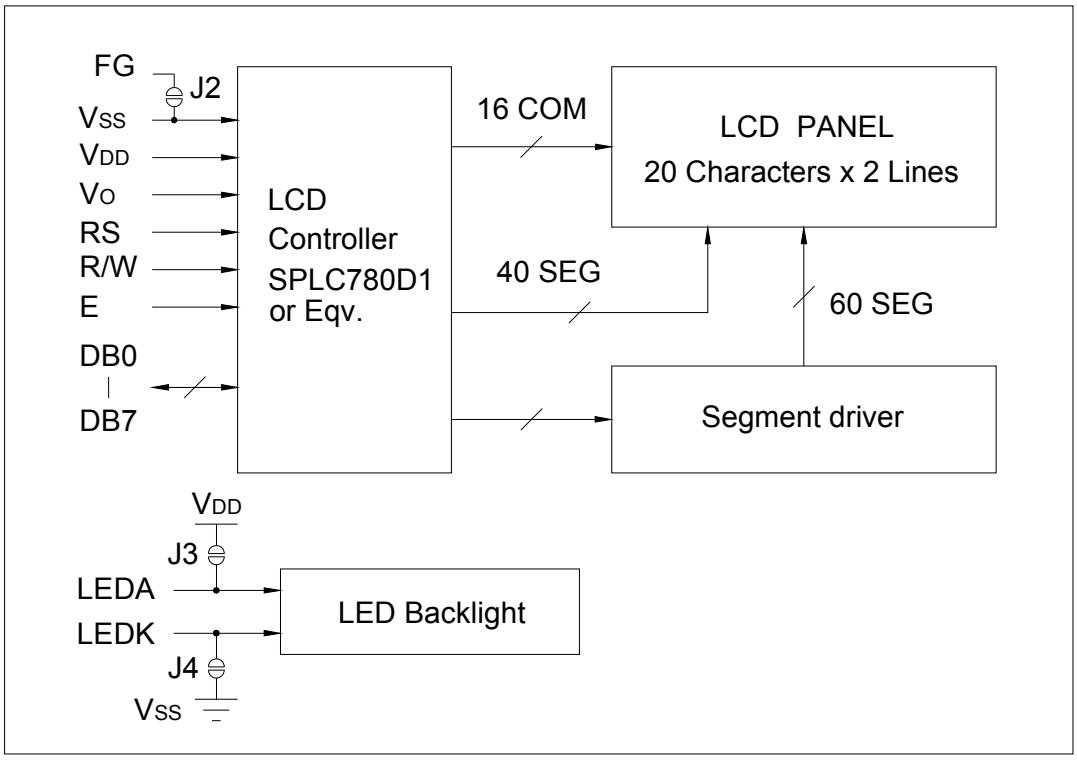
Rev.	Date	Page	Item	Description
0.1	2009/06/25	-	-	New release
0.2	2011/10/26	All pages	-	Change content organization.
1.0	2013/12/02	3 22	1.4 8	1. Add section 1.4: Swap Pin15/Pin16 terminal functions 2. Change PCB width from 37.0mm to 35.0mm.
1.1	2016/01/26	6	3.3, 3.4	Modify LED backlight characteristics and power supply circuit

1. BASIC SPECIFICATIONS

1.1 Features

Item	Specifications	Unit
Display Format	20 Characters x 2 Lines	-
LCD Type	STN - Blue - Negative - Transmissive White characters on blue background	-
Driving Method	1/16 Duty, 1/4 Bias	-
Viewing Direction	6	O'clock
Backlight & Color	LED, white color	-
Outline Dimension (WxHxT)	116.0 x 35.0 x 13.5	mm
Viewing Area (WxH)	83.0 x 18.6	mm
Character Size (WxH)	3.20 x 5.55	mm
Dot Size (WxH)	0.60 x 0.65	mm
Weight	55	g
Controller	SPLC780D1-001A	-
Interface	8-bit parallel (6800 series MPU)	-
Power Supply (VDD)	2.7 to 5.5	V

1.2 Block Diagram



1.3 Terminal Functions

Pin No.	Symbol	Level	Function
1	VSS	0V	Ground (connects to frame ground via jumper J2)
2	VDD	2.7V to 5.5V	Power supply for logic
3	VO	-	Operating voltage for LCD (contrast adjusting). Refer to section 3.5
4	RS	H/L	Data or instruction selection H: Display data L: Instruction code
5	R/W	H/L	Read or write selection H: Read operation L: Write operation
6	E	H, H→L	Enable signal In read mode (R/W="H"), data appears at DB0 to DB7 while E is "H". In write mode (R/W="L"), data of DB0 to DB7 is latched at the falling edge of E.
7	DB0	H/L	In 8-bit mode, used as low order bi-directional data bus. In 4-bit mode, open these terminals.
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	In 8-bit mode, used as high order bi-directional data bus. In 4-bit mode, used as both high and low order data bus.
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	
15	LEDA	5V	Power supply for LED backlight Refer to section 1.4, 3.3, 3.4
16	LEDK	0V	

1.4 Swap Pin 15 and Pin 16 Terminal Functions

Jumper Status		Terminal Functions		Remark
J5, J8	J6, J7	Pin 15	Pin 16	
Close	Open	LEDA	LEDK	**<Default>**
Open	Close	LEDK	LEDA	

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Supply Voltage (Logic)	VDD-VSS	-0.3	7.0	V
Supply Voltage (LCD)	VDD-VO	-0.3	10.0	V
Input Voltage	VI	-0.3	VDD+0.3	V
Operating Temperature	Topr	-20	70	°C
Storage Temperature	Tstg	-30	80	°C

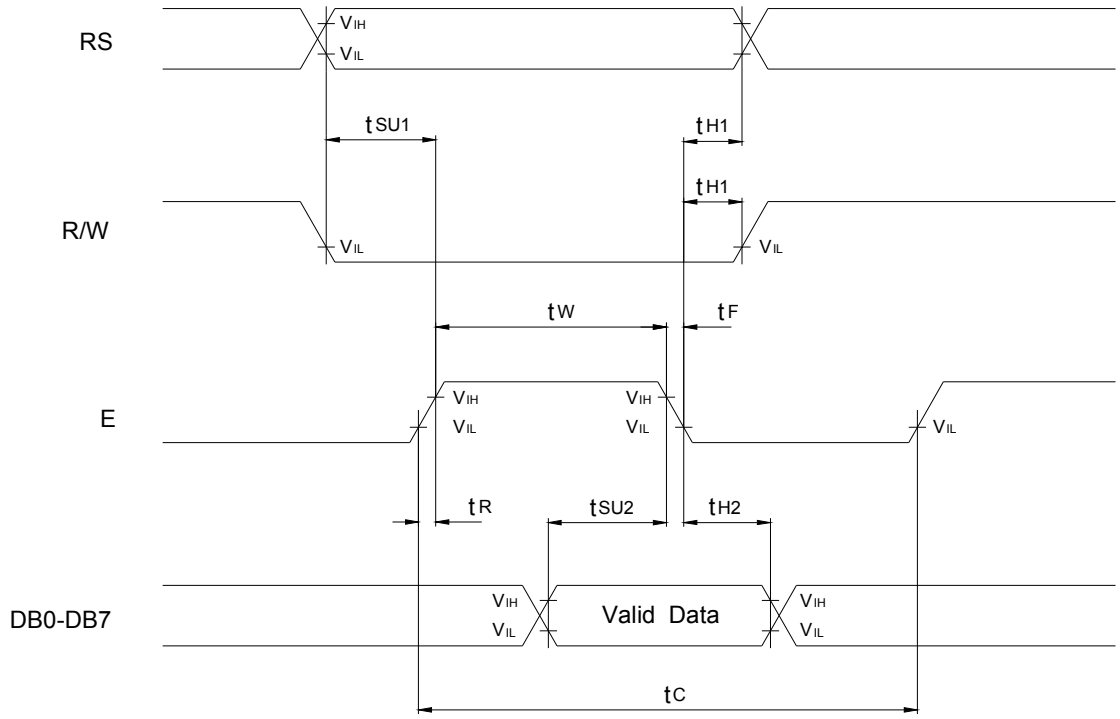
3. ELECTRICAL CHARACTERISTICS

3.1 DC Characteristics (Ta=25°C)

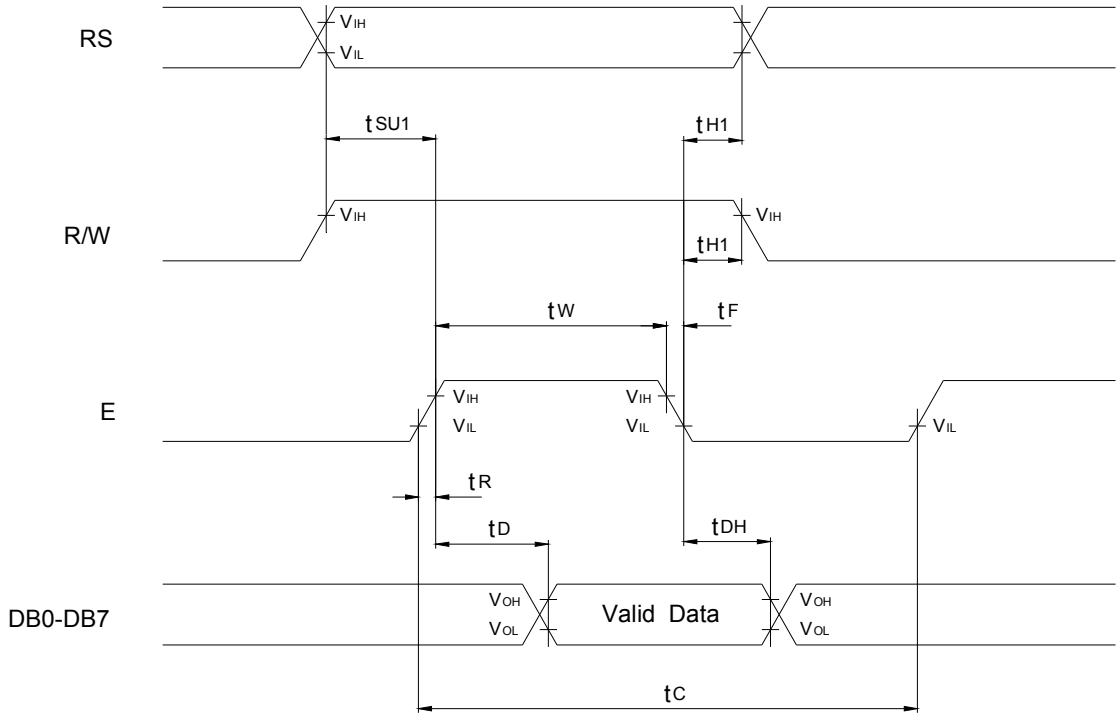
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (Logic)	VDD		2.7	5.0	5.5	V
Supply Voltage (LCD Drive)	VDD-VO		-	4.6	-	V
Input High Voltage	VIH	VDD=4.5 to 5.5V	2.5	-	VDD	V
		VDD=2.7 to 4.5V	0.7VDD	-	VDD	V
Input Low Voltage	VIL	VDD=4.5 to 5.5V	-0.3	-	0.6	V
		VDD=2.7 to 4.5V	-0.3	-	0.55	V
Output High Voltage	VOH	VDD=4.5 to 5.5V IOH=-0.1mA	2.4	-	VDD	V
		VDD=2.7 to 4.5V IOH=-0.1mA	0.75VDD	-	VDD	V
Output Low Voltage	VOL	VDD=4.5 to 5.5V IOH=0.1mA	0	-	0.4	V
		VDD=2.7 to 4.5V IOH=0.1mA	0	-	0.2VDD	V
Supply Current (Logic)	IDD	VDD=5.0V	-	1.6	3.0	mA

3.2 Interface Timing Chart (Ta=25°C)

Mode	Characteristic	Symbol	VDD=4.5 to 5.5V		VDD=2.7 to 4.5V		Unit
			Min.	Max.	Min.	Max.	
Write Mode (Refer to MPU Write Timing)	E Cycle Time	t_C	400	-	1000	-	ns
	E Rise/Fall Time	t_R, t_F	-	25	-	25	
	E Pulse Width (High,Low)	t_W	150	-	450	-	
	R/W and RS Setup Time	t_{SU1}	30	-	60	-	
	R/W and RS Hold Time	t_{H1}	10	-	20	-	
	Data Setup Time	t_{SU2}	40	-	195	-	
	Data Hold Time	t_{H2}	10	-	10	-	
Read Mode (Refer to MPU Read Timing)	E Cycle Time	t_C	400	-	1000	-	ns
	E Rise/Fall Time	t_R, t_F	-	25	-	25	
	E Pulse Width (High,Low)	t_W	150	-	450	-	
	R/W and RS Setup Time	t_{SU}	30	-	60	-	
	R/W and RS Hold Time	t_H	10	-	20	-	
	Data Output Delay Time	t_D	-	100	-	360	
	Data Hold Time	t_{DH}	5	-	5	-	



MPU Write Timing

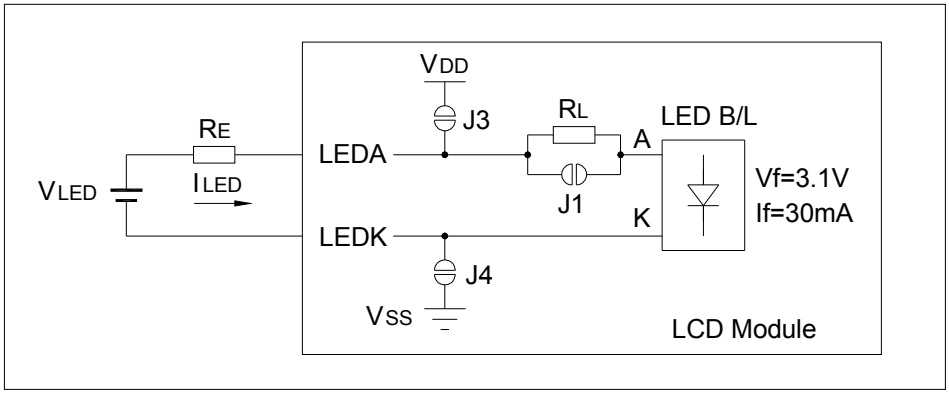


MPU Read Timing

3.3 LED Backlight Characteristics (Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage	Vf		2.9	3.1	3.3	V
Forward Current	If	Vf=3.1V	-	30	-	mA
Color	White					

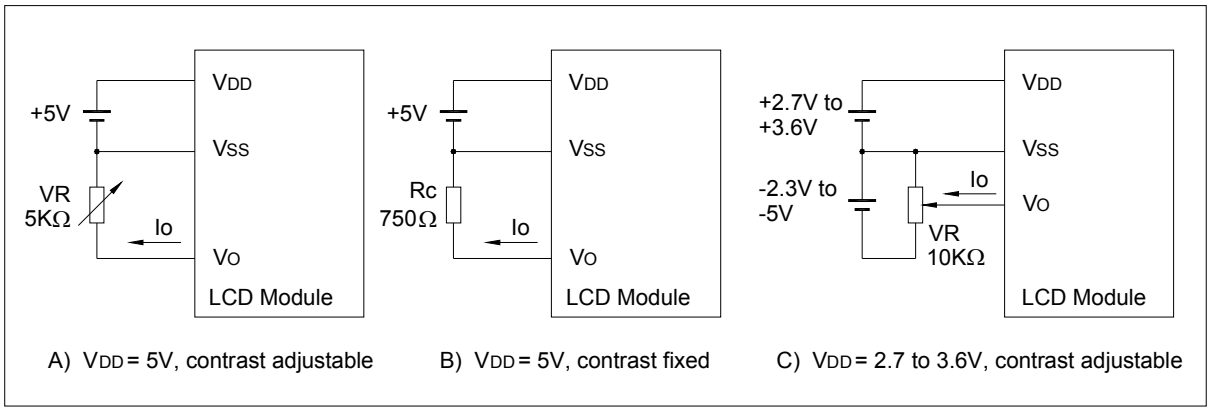
3.4 Power Supply for LED Backlight



RL (internal) and RE (external) are the current limiting resistors for LED backlight

VLED	Jumper Status	RE Values	Remark
5V	J1, J3, J4 open	0Ω	Default
Higher than 5V	J1, J3, J4 open	(VLED – 5.0V)/30mA	
Lower than 5V	J1 close; J3, J4 open	(VLED – 3.1V)/30mA	
Open	J1 open; J3, J4 close	Open	Driving LED backlight from VDD (5V) and VSS

3.5 Power Supply for Logic and LCD Driving



VO is LCD driving voltage (contrast adjusting). Adjust VDD-VO to be around 4.6V for better contrast.

4. OPERATING PRINCIPLES & METHODS

4.1 Register

The LCD controller has two 8-bit registers, the Instruction register (IR) and the data register (DR).

The IR is a write only register to store instruction codes like Display Clear or Cursor Shift as well as addresses for the Display Data RAM (DDRAM) or the Character Generator RAM (CGRAM).

The DR is a read/write register used for temporarily storing data to be read/written to/from the DDRAM or CGRAM. Data written into the DR is automatically written into DDRAM or CGRAM by an internal operation of the display controller.

The DR is also used to store data when reading out data from DDRAM or CGRAM. When address information is written into IR, data is read out from DDRAM or CGRAM to DR by an internal operation. Data transfer is then completed by reading the DR.

After performing a read from the DR, data in the DDRAM or CGRAM at the next address is sent to the DR for the next read cycle. The register select (RS) signal determines which of these two registers is selected.

Table 4.1 Selection of Registers

RS	R/W	Function
0	0	Instruction Write operation (MPU writes instruction code to IR)
	1	Read Busy flag (DB7) and Address Counter (DB0 to DB6)
1	0	Data Write operation (MPU writes data to DR)
	1	Data Read operation (MPU reads data from DR)

4.2 Busy Flag (BF)

When the busy flag is high or “1” the module is performing an internal operation and the next instruction will not be accepted. The busy flag outputs to DB7 when RS = 0 and a read operation is performed. The next instruction must not be written until ensuring that the busy flag is low or “0”.

4.3 Address Counter (AC)

The address counter (AC) assigns addresses to the DDRAM and the CGRAM.

When the address of an instruction is written into the IR, the address information is sent from the IR to the AC. The selection of either DDRAM or CGRAM is also determined concurrently by the same instruction. After writing into or reading from the DDRAM or CGRAM the address counter (AC) is automatically increased by 1 or decreased by 1 (determined by the I/D bit in the “Entry Mode Set” command). AC contents are output to DB0 to DB6 when RS = 0 and a read operation is performed.

4.4 Display Data RAM (DDRAM)

The Display Data RAM (DDRAM) stores the display data represented in 8-bit character codes. Its capacity is 80 x 8 bits or 80 characters. The Display Data RAM that is not used for the display can be used as a general data RAM.

The DDRAM address (ADD) is set in the Address Counter (AC) and is represented in hexadecimal. The address counter can be written by using the “Set DDRAM Address” instruction and can be read by using the “Read Busy Flag and Address” instruction. In each case, data bits DB0 to DB6 represent the DDRAM address. In the read operation, bit DB7 represents the “Busy Flag”.

MSB							LSB
BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Relations between DD RAM addresses and positions on the liquid crystal display are shown below.

Display position →		1	2	3	---	18	19	20
DD RAM Addr.	Line 1	00H	01H	02H	---	11H	12H	13H
	Line 2	40H	41H	42H	---	51H	52H	53H

When display shift operation is performed, the DD RAM address moves as follows:
For left shift:

Display position →		1	2	3	---	18	19	20
DD RAM Addr.	Line 1	01H	02H	03H	---	12H	13H	14H
	Line 2	41H	42H	43H	---	52H	53H	54H

For right shift:

Display position →		1	2	3	---	18	19	20
DD RAM Addr.	Line 1	27H	00H	01H	---	10H	11H	12H
	Line 2	67H	40H	41H	---	50H	51H	52H

4.5 Character Generator ROM (CGROM)

The Character Generator ROM (CGROM) generates 5 x 7 dot or 5 x 10 dot character patterns from 8-bit character codes. It can generate up to 192 types of 5x7 dot character patterns and 32 types of 5x10 dot character patterns. Table 4.3 shows the relation between character codes and character patterns of the standard character font.

4.6 Character Generator RAM (CGRAM)

The CGRAM is a 64 x 8 bit RAM in which the user can program custom character patterns. With 5 x 7 dots, 8 types of character patterns can be written and with 5 x 10 dots 4 types of character patterns can be written. To write previously programmed characters from the CGRAM to the DDRAM, character codes 00H through 07H are used. (See character font Table 4.3). Unused CGRAM locations can be used for general purpose RAM.
The relationship between CGRAM address and data and the displayed character is shown in Tables 4.2

To program a 5 x 7 character pattern into the CGRAM location (for example, character code 01H), the following steps should be taken.

A. Use the “Set CGRAM address” command to position the CGRAM pointer to the 1st row of character code 01H (CGRAM address=48H).
B. Use the “Write Data to CG or DDRAM” Command to write the top row of the custom character (Only lower 5-bit of character pattern data is valid).
C. The CGRAM address is automatically increased if the I/D bit is set in the “Entry Mode Set” command. When this is the case, return to step B until all rows of the character are written.
D. After writing all 7 rows of data, use the “Set DDRAM address” command to return the address counter to a DDRAM location.
E. To display the custom character written above, use the “Write Data to CG or DDRAM” command with the data being 01H to display the character in the DDRAM address.

Table 4.2 Relationship between CGRAM address, Character Codes (DDRAM Data) and Character Patterns (CGRAM Data)

(5x8 dots character patterns)

Character Code (DDRAM Data)	CGRAM Address	CGRAM Data	Pattern No.
D7 D6 D5 D4 D3 D2 D1 D0	A5 A4 A3 A2 A1 A0	P7 P6 P5 P4 P3 P2 P1 P0	
0 0 0 0 x 0 0 0	0 0 0 0 0 0	x x x 0 1 1 1 0	Pattern 1
	0 0 1	x x x 1 0 0 0 1	
	0 1 0	x x x 1 0 0 0 1	
	0 1 1	x x x 1 1 1 1 1	
	1 0 0	x x x 1 0 0 0 1	
	1 0 1	x x x 1 0 0 0 1	
	1 1 0	x x x 1 0 0 0 1	
	1 1 1	x x x 0 0 0 0 0	Cursor
. . . . .	. . . . .	. . . . .	. . . . .
0 0 0 0 x 1 1 1	0 0 0 0 0 0	x x x 1 0 0 0 1	Pattern 8
	0 0 1	x x x 1 0 0 0 1	
	0 1 0	x x x 1 0 0 0 1	
	0 1 1	x x x 1 1 1 1 1	
	1 0 0	x x x 1 0 0 0 1	
	1 0 1	x x x 1 0 0 0 1	
	1 1 0	x x x 1 0 0 0 1	
	1 1 1	x x x 0 0 0 0 0	Cursor

Notes:

1. Character code bits 0 to 2 correspond to CGRAM address bit 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the line position within a character pattern. The 8th line is the cursor position and display is determined by the logical OR of the 8th line and the cursor. Maintain the 8th line data, corresponding to the cursor display position, in the “0” state for cursor display. When the 8th line data is “1”, bit 1 lights up regardless of cursor existence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 as shown in the above (bit 4 being at the left end). Since CGRAM data bits 5 to 7 are not used for display, they can be used for the general data RAM as memory elements still exit.
4. As shown in Table 4.2, CGRAM character patterns are selected when character code bits 4 to 7 are all “0”. However as character code bit 3 is an ineffective bit, the “A” in the character pattern example is selected by character code “00H” or “08H”.
5. “1” for CGRAM data corresponds to selected pixels and “0” for non-selected.

Table 4.3 CGROM Character Code Table (SPLC780D1-001A)



5. MPU INTERFACE

5.1 General

(1). The LCD controller can be operated in either 4 or 8 bits mode. Instructions/Data are written to the display using the signal timing characteristics found in section 3.2.
When operating in 4-bit mode, data is transferred in two 4-bit operations using data bits DB4 to DB7. DB0 to DB3 are not used. When using 4-bit mode, data is transferred twice before the instruction cycle is complete. The higher order 4 bits (contents of DB4 to DB7 when interface data is 8 bits long) is transferred first, then the lower order 4 bits (contents of DB0 to DB3 when interface data is 8 bits long) is transferred. Check the busy flag after 4-bit data has been transferred twice (one instruction). A 4-bit two operation will then transfer the busy flag and address counter data.
(2). When operating in 8-bit mode, data is transferred using the full 8-bit bus DB0 to DB7.

5.2 Initialization

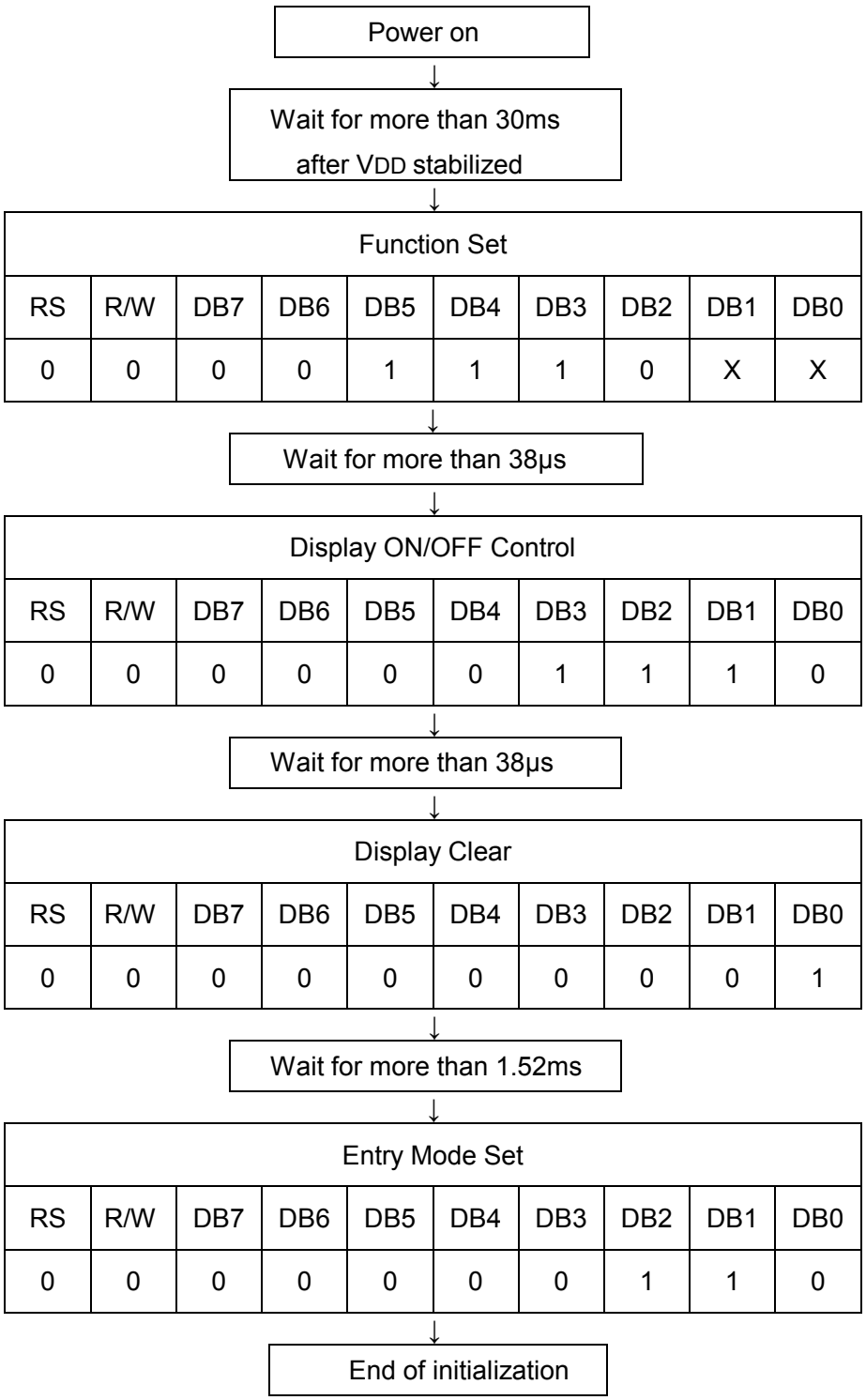
5.2.1 Initialization by the Internal Reset Circuit

The display can be initialized using the internal reset circuit when the power is turned on. The following instructions are executed in initialization. The busy flag (BF) is kept in busy state until initialization ends. The busy flag will go active 10ms after V_{DD} rises to 4.5V.
(1). Display Clear
(2). Function set:
DL = 1 : 8 bit interface operation
N = 0 : 1 - line display mode
F = 0 : 5 x 7 dots character font
(3). Display ON/OFF Control:
D = 0 : Display OFF
C = 0 : Cursor OFF
B = 0 : Blink OFF
(4). Entry Mode Set
I/D = 1 : +1 (Increment Mode)
SH = 0 : No Display Shift operation
If the internal power supply reset timing cannot be met (0.1ms<trcc<10ms), the internal reset circuit will not operate normally and initialization will not be performed. In this case, the display must be initialized by software.

5.2.2 Software Initialization

Although software initialization is not mandatory, it is recommended that this procedure always be performed. When the internal power supply reset timing cannot be met, then the display must be initialized using one of the following procedures.

(1) 8-Bit Initialization:



(2) 4-Bit Initialization:

Power on

↓

Wait for more than 30ms after V_{DD} stabilized

↓

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	X	X	X	X
0	0	0	0	1	0	X	X	X	X
0	0	1	0	X	X	X	X	X	X

↓

Wait for more than 38μs

↓

Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	1	1	1	0	X	X	X	X

↓

Wait for more than 38μs

↓

Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	0	0	1	X	X	X	X

↓

Wait for more than 1.52ms

↓

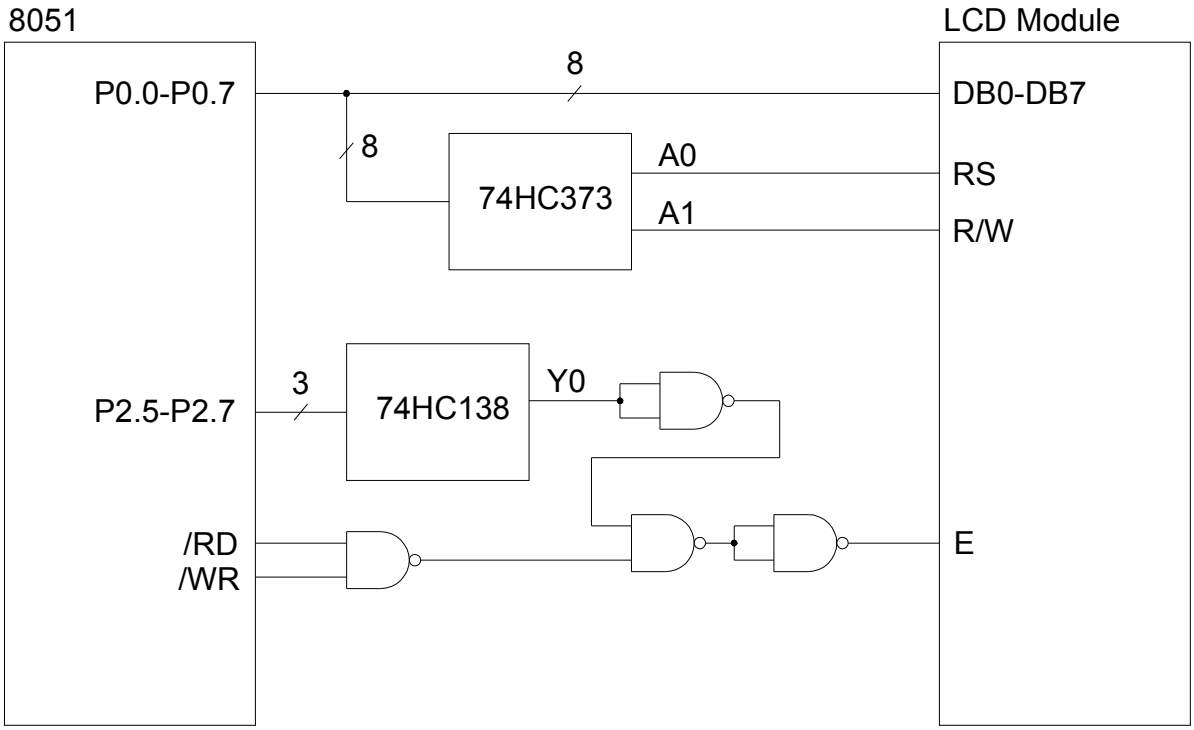
Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	1	1	0	X	X	X	X

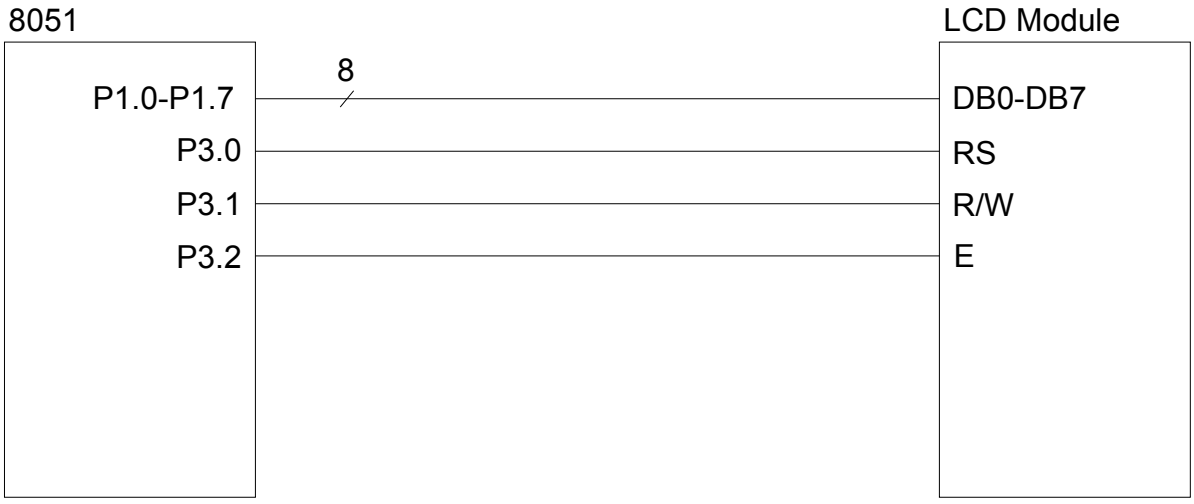
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End of initialization

5.3 Connection with 8051 Family MPU



a. Application Circuit 1



b. Application Circuit 2

6. DISPLAY CONTROL INSTRUCTIONS

Table 6.1 Instructions

Instruction	Instruction code										Description	Execution time (fosc=270KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear entire display and set DDRAM address to 00H.	1.52ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to 00H in AC and return shifted display to its original position. The contents of DDRAM remain unchanged.	1.52ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Set cursor move direction and enable the shift of entire display. These operations are performed during data write and read.	38μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set ON/OFF of entire display (D), cursor ON/OFF (C), and blinking of cursor position character (B).	38μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Move cursor and shift display without changing DDRAM contents.	38μs
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line), and display font type (F: 5x11dots/5x8dots)	38μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	38μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	38μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read busy flag (BF) indicating internal operation status. The contents of address counter can also be read.	0μs
Write data to CGRAM or DDRAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	38μs
Read data from CG or DDRAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	38μs

"-": don't care

Notes:

1. Make sure to check the busy flag before sending the instruction to the display. If the busy flag is not checked, the time between first and next instruction must be longer than the instruction execution time list in the Table 6.1.
2. After execution of CGRAM/DDRAM data write or read instruction, the RAM address counter is increased or decreased by 1. The RAM address counter is updated after the busy flag turns off.

6.1 Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing the space code “20H” to all DDRAM addresses, and set DDRAM address to “00H” into address counter. Return cursor to the original position, namely, bring the cursor to the upper left end of the display. The execution of clear display instruction sets entry mode to increment mode (I/D = 1).

6.2 Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Set the DDRAM address “00H” in address counter. Return display to its original position if it was shifted. DDRAM contents do not change. The cursor or the blink moves to the upper left end of the display. Contents of DDRAM remain unchanged.

6.3 Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the move direction of cursor and display.

I/D: Increase (I/D = 1) or decrease (ID = 0) the DDRAM address by 1 when a character code is written into or read from the DDRAM.
The cursor or blink moves to the right when increased by 1 and to the left when decreased by 1. The same applies to writing and reading the CGRAM.

SH: Shift the entire display when SH = 1; shift to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and only the display seems to move. The display does not shift when reading from DDRAM or writing/reading into/from CGRAM.
When SH = 0, the display does not shift.

6.4 Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control the display ON/OFF status, Cursor ON/OFF and Cursor Blink function.

D: The entire display is ON when D = 1 and OFF when D = 0. The display data remains in the DDRAM when display is OFF, it can be displayed immediately by setting D = 1.

C: The cursor displays when C = 1 and does not display when C = 0. The cursor is displayed on the 8th line when 5x7 dots character font has been selected.

B: The character indicated by the cursor blinks when B = 1. The blink is displayed by switching between all “High” data and display characters at 0.4 sec intervals. The cursor and the blink can be set to display simultaneously. When B = 0, the blink is off.

6.5 Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shift the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display.

Note that the display shift is performed simultaneously in all lines.

The contents of address counter do not change when display shift is performed.

Table 6.2 Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shifts cursor position to the left (AC is decreased by 1)
0	1	Shifts cursor position to the right (AC is increased by 1)
1	0	Shifts the entire display to the left, cursor follows the display shift.
1	1	Shifts the entire display to the right, cursor follows the display shift.

6.6 Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

Set the interface data length, the number of lines, and character font.

DL: Set interface data length. Data is sent or received in 8-bit length (DB7 to DB0) when DL = 1, and in 4-bit length (DB7 to DB4) when DL = 0. When the 4-bit length is selected, data must be sent or received twice.

N: Set the number of lines

N = 0 : 1 line display (1/8 duty)

N = 1 : 2 lines display (1/16 duty)

F: Set character font.

F = 0 : 5 x 7 dots

F = 1 : 5 x 10 dots

Note: Perform the function at the head of the program before executing all instructions (except Busy flag/address read).

6.7 Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set the CGRAM address to the address counter. Data is then written/read to/from the CGRAM.

6.8 Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set the DDRAM address to the address counter. Data is then written/read to/from the DDRAM.

When in 1-line display mode (N = 0), DDRAM address is from “00H” to “4FH”.

When in 2-line display mode (N = 1), DDRAM address corresponding to 1st line and 3rd line of the display is from “00H” to “27H”; the address corresponding to 2nd and 4th line of the display is from “40H” to “67H”.

6.9 Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Read the busy flag (BF) and value of the address counter (AC). BF = 1 indicates that internal operation is in progress and the next instruction will not be accepted until BF is set to “0”. The BF status should be checked before each write operation. At the same time the value of the address counter is read out. The address counter is used by both CGRAM and DDRAM and its value is determined by the previous instruction.

6.10 Write Data to CGRAM or DDRAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to the CGRAM or DDRAM.
The previous address set instruction (CGRAM address set or DDRAM address set) determines whether the CGRAM or DDRAM is to be written. After a write the address is automatically increased or decreased by 1, according to the entry mode. The entry mode also determines display shift.

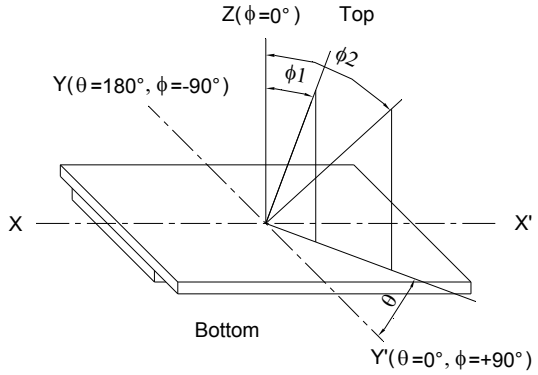
6.11 Read Data from CGRAM or DDRAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

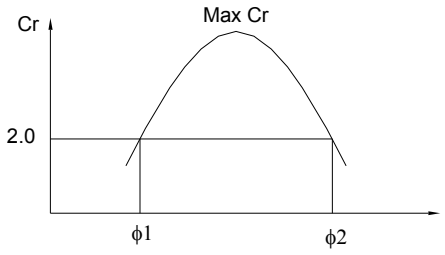
Read binary 8-bit data from the CGRAM or DDRAM.
The previous address set instruction (CGRAM address set or DDRAM address set) determines whether the CGRAM or DDRAM is to be read. Before entering the read instruction, you must execute either the CGRAM or DDRAM address set instruction. If you don't, the first read data will be invalidated. If RAM data is read several times without RAM address instruction set before read operation, the correct RAM data can be obtained from the second read. The "address set" instruction need not be executed just before the "read" instruction when shifting the cursor by cursor shift instruction (when reading DDRAM). The cursor shift instruction operation is the same as that of the DDRAM address set instruction.
After a read the address is automatically increased or decreased by 1, according to the entry mode; however, display shift is not executed no matter what the entry mode is.
Note: The address counter (AC) is automatically increased or decreased by 1 after a "write" instruction to either CGRAM or DDRAM. RAM data selected by the AC cannot then be read out even if "read" instructions are executed.
The conditions for correct data read out are: (a) Execute either the address set instruction or cursor shift instruction (only with DDRAM) or (b) The execution of the "read data" instruction from the second time when the read instruction is performed multiple times in serial.

7. ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

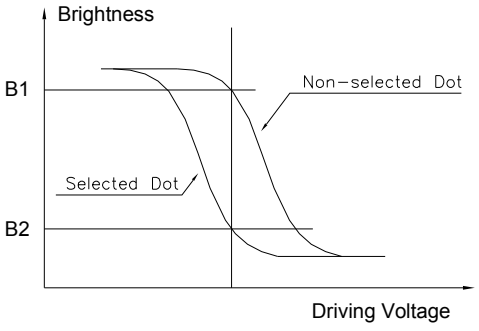
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
View Angle	Φ2-Φ1	Cr≥2 , θ=0°	-	80	-	Deg	Note1, Note2
Contrast Ratio	Cr	Φ=0°,θ=0°	3	-	-	-	Note3
Response Time	tr (rise)	Φ=0°,θ=0°	-	200	-	ms	Note4
	tf (fall)	Φ=0°,θ=0°	-	250	-	ms	



Note1: Definition of viewing angle ϕ, θ

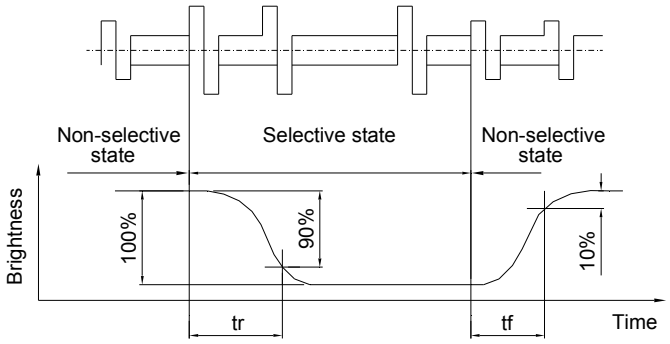


Note2: Definition of viewing angle range ϕ1, ϕ2



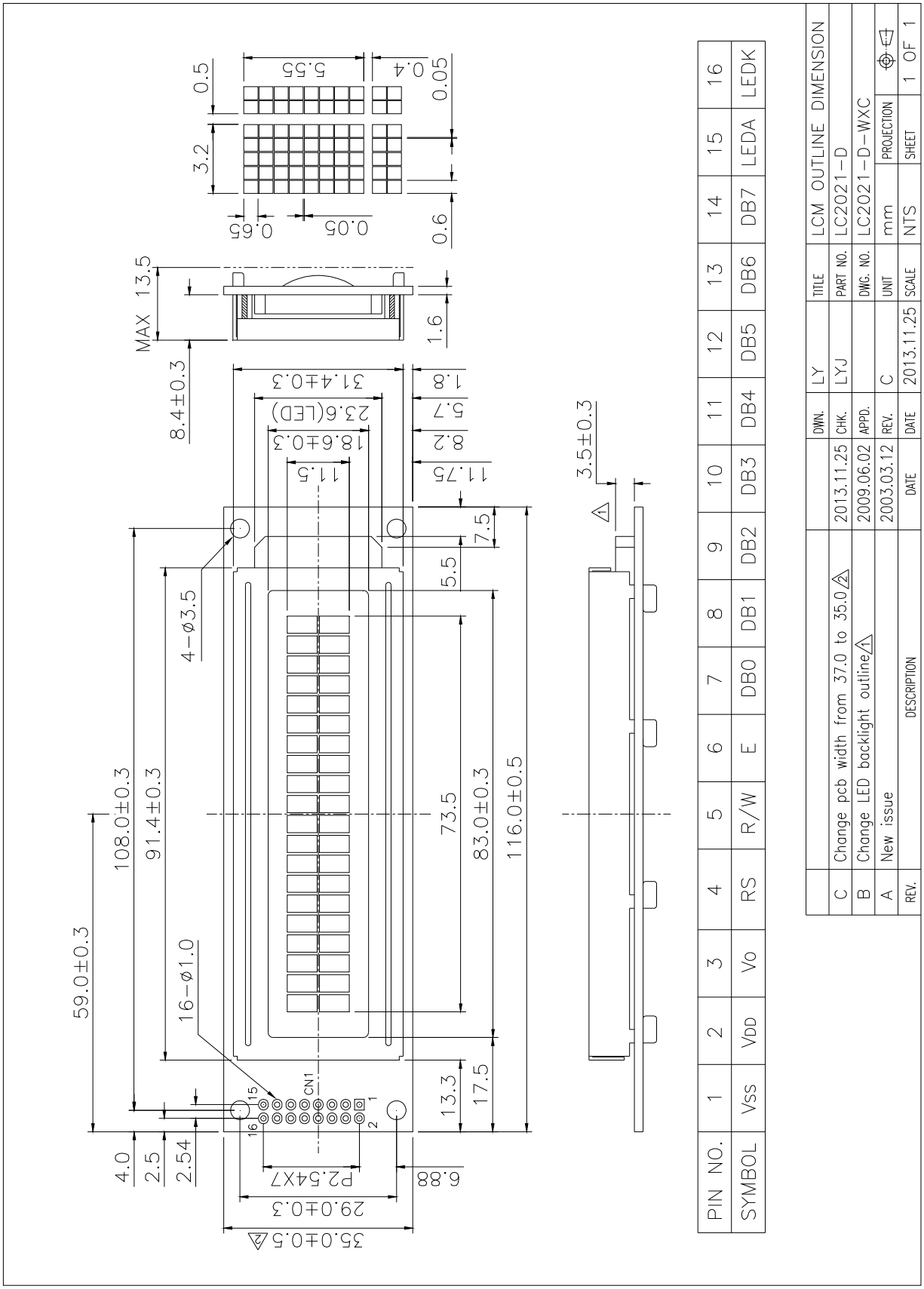
$$\text{Contrast Ratio} = \frac{\text{Brightness of non-selected dot (B1)}}{\text{Brightness of selected dot (B2)}}$$

Note3: Definition of contrast ratio (positive type)



Note3: Definition of response time

8. DIMENSIONAL OUTLINE



9. LCD MODULE NUMBERING SYSTEM

L	C	20	2	1	-	B	M	D	W	H	6	N	-	D
(1)	(2)	(3)	(4)	(5)		(6)	(7)	(8)	(9)	(10)	(11)	(12)		(13)

(1) Brand

(2) Module type

C - Character module

G - Graphic module

(3) Display format

Character module : Number of characters per line, two digits XX

Graphic module : Number of columns, three digits XXX

(4) Display format

Character module : Number of lines, one digit X

Graphic module : Number of rows, two or three digits XX or XXX

(5) Development number : One or two digits X or XX

(6) LCD mode

T - TN Positive, Gray **N** - TN Negative, Blue

S - STN Positive, Yellow green **G** - STN Positive, Gray

B - STN Negative, Blue **F** - FSTN Positive, White

K - FSTN Negative, Black **L** - FSTN Negative, Blue

Q - FFSTN Negative, Black

(7) Polarizer mode

R - Reflective **F** - Transflective **M** - Transmissive

(8) Backlight type

N - Without backlight **L** - Array LED **D** - Edge-lit LED **E** - EL **C** - CCFL

(9) Backlight color

Y - Yellow green **B** - Blue **W** - White **G** - Green

A - Amber **R** - Red **M** - Multi color **N or Nil** - Without backlight

(10) Operating temperature range

S - Standard temperature (0 to +50 ^{o}C) **H** - Extended temperature (-20 to +70 ^{o}C)

(11) Viewing direction

3 - 3:00 **6** - 6:00 **9** - 9:00 **U** - 12:00

(12) DC-DC Converter

N or Nil - Without DC-DC converter **V** - Built in DC-DC converter

(13) Version code

D - SPLC780D1-001A LCD controller

10. PRECAUTIONS FOR USE OF LCD MODULE

10.1 Handing Precautions

1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
2) If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth. If the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.
3) Do not apply excessive force on the surface of display or the adjoining areas of LCD module since this may cause the color tone to vary.
4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
5) If the display surface of LCD module becomes contaminated, blow on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents.
   · Isopropyl alcohol
   · Ethyl alcohol
   Solvents other than those mentioned above may damage the polarizer.
   Especially, do not use the following:
   · Water
   · Ketone
   · Aromatic Solvents
6) When mounting the LCD module make sure that it is free of twisting, warping, and distortion. Distortion has great influence upon display quality. Also keep the stiffness enough regarding the outer case.
7) Be sure to avoid any solvent such as flux for soldering never stick to Heat-Seal. Such solvent on Heat-Seal may cause connection problem of heat-Seal and TAB.
8) Do not forcibly pull or bend the TAB I/O terminals.
9) Do not attempt to disassemble or process the LCD module.
10) NC terminal should be open. Do not connect anything.
11) If the logic circuit power is off, do not apply the input signals.
12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
   · Be sure to ground the body when handling the LCD module.
   · Tools required for assembly, such as soldering irons, must be properly grounded.
   · To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
   · The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

1) When storing the LCD module, avoid exposure to direct sunlight or to the light of fluorescent lamps and high temperature/high humidity. Whenever possible, the LCD module should be stored in the same conditions in which they were shipped

from our company.

2) Exercise care to minimize corrosion of the electrodes. Corrosion of the electrodes is accelerated by water droplets or a current flow in a high humidity environment.

10.3 Design Precautions

1) The absolute maximum ratings represent the rated value beyond which LCD module can not exceed. When the LCD modules are used in excess of this rated value, their operating characteristics may be adversely affected.
2) To prevent the occurrence of erroneous operation caused by noise, attention must be paid to satisfy VIL, VIH specification values, including taking the precaution of using signal cables that are short.
3) The liquid crystal display exhibits temperature dependency characteristics. Since recognition of the display becomes difficult when the LCD is used outside its designated operating temperature range, be sure to use the LCD within this range. Also, keep in mind that the LCD driving voltage levels necessary for clear displays will vary according to temperature.
4) Sufficiently notice the mutual noise interference occurred by peripheral devices.
5) To cope with EMI, take measures basically on outputting side.
6) If DC is impressed on the liquid crystal display panel, display definition is rapidly deteriorated by the electrochemical reaction that occurs inside the liquid crystal display panel. To eliminate the opportunity of DC impressing, be sure to maintain the AC characteristics of the input signals sent to the LCD Module.

10.4 Others

1) Liquid crystals solidify under low temperatures (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white).
   Air bubbles may also be generated if the LCD module is subjected to a strong shock at a low temperature.
2) If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.
3) To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity, etc., exercise care to avoid touching the following sections when handling the module:
   · Terminal electrode sections.
   · Part of pattern wiring on TAB, etc.