aTS75

LOW-VOLTAGE 2-WIRE DIGITAL TEMPERATURE SENSOR With Thermal Alarm

Fully Released Specification

PRODUCT SPECIFICATION

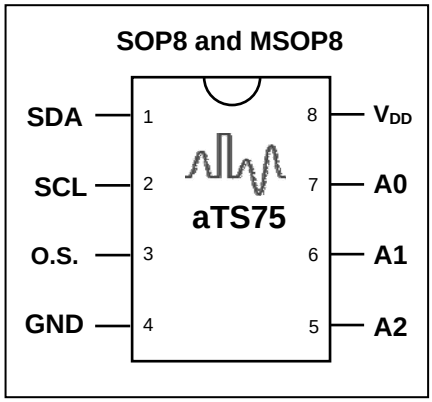
Product Description

The aTS75 is a CMOS temperature sensor with a Delta-Sigma temperature-to-digital converter and a SMBus compatible serial digital interface. The aTS75 is accurate to ±2° at 25°C and to ±3°C over the range of 0°C to 100°C. The aTS75 provides digital temperature data with 9- to 12-bit resolution. The default resolution is 9-bits, but for applications requiring higher resolution, the user can program the aTS75 to provide 10-, 11-, or 12-bit data.

The aTS75 features a thermal alarm function with a user-programmable trip temperature and turn-off temperature. This alarm can operate in two modes — interrupt mode and comparator mode — which allows flexibility for many types of applications.

The aTS75 is available in SOIC-8 and MSOP-8 surface mount packages.

Pin Configuration



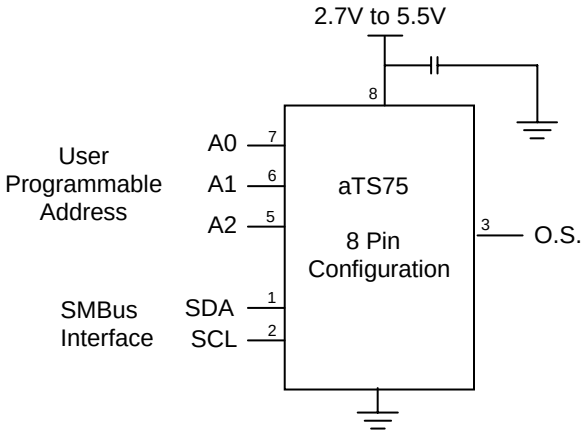
Features

User Configurable to 9-, 10-, 11-, or 12-bit Resolution
Calibrated to ±3°C from 0°C to 100°C
Temperature Range: -30°C to 125°C
Low Operating Current (less than 250μA)
Low Self Heating (0.2°C max in still air)
Operating Voltage Range: 2.7V to 5.5V

Applications

Battery Management
FAX Management
Printers
Portable Medical Instruments
HVAC
Power Supply Modules
Disk Drives
Computers
Automotive

Application Diagram



Ordering Information

Part Number	Package	Temperature Range	Marking	How Supplied
aTS75D8	8-Lead SOIC	-30°C to 125°C	aTS75 AYWW	2500 units Tape & Reel
aTS75M8	8-Lead MSOP	-30°C to 125°C	TS75 AYWW	2500 units Tape & Reel

AYWW – assembly site code, last digit of year, workweek

Absolute Maximum Ratings[1]

Parameter		Rating
Supply Voltage		+7V
Output Voltage		V_{CC} + 0.5V
Continuous Current, any terminal		10mA
Storage Temperature Range		-60°C to +150°C
Lead Soldering Temperature		220°C
ESD[2]	Human Body Model	Class 1B
	Machine Model	Class A
	Charged Device Model	Class IV

Electrical Characteristics[3]

(-30°C≤T_A≤+125°C, VCC=5.0V unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Specified Temperature Range	T_{MIN}, T_{MAX}		-30	—	+125	°C
Temperature Conversion Time[4]				90		ms
Accuracy[5]		T_A= 0°C	-3	—	+3	°C
		T_A=+25°C	-2	—	+2	°C
		T_A=+100°C	-3	—	+3	°C
		T_A = -30°C (T_{MIN})	-4	—	+4	°C
		T_A=+125°C (T_{MAX})	-4	—	+4	°C

Logic Electrical Characteristics (T_A = 25 °C, V_{DD} = 5V unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Min Input Voltage Logic High	V_{IH}		V_{DD} X 0.7		V_{DD} + 0.5	V
Max Input Voltage Logic Low	V_{IL}		-0.3		V_{DD} X 0.3	V
Max Output Voltage Logic Low	V_{OL}	V_{DD}= 5V, I_{OL} = -3mA			0.36	V
		V_{DD}= 3V, I_{OL} = -1.5mA			0.36	
Quiescent Supply Current	I_{DD}	Interface Inactive		220	250	µA
		R/W Activity on SDA		350	500	
Shutdown Current	I_{DD-SD}	Interface Inactive		0.15	1	µA
		R/W Activity on SDA		83	150	
Input Leakage Current	I_{IN}	V_{IN} = 0V or 5V, T_A = 25 °C			±0.1	µA
		-40°C < T_A < 125 °C			±1.0	
Output Sink Current	I_{OL}	T_A = 25 °C, V_{OL} = 0.4V			3	mA
Output Leakage Current	I_{LEAK}	V_{OH} = 5V, V_{DD} = 0V		0.001	5	µA
Output Transition Time	t_F	C_L= 400pF, I_{OL} = -3mA			250	ns
Input Capacitance	C_{IN}	All Digital Inputs			20	pF

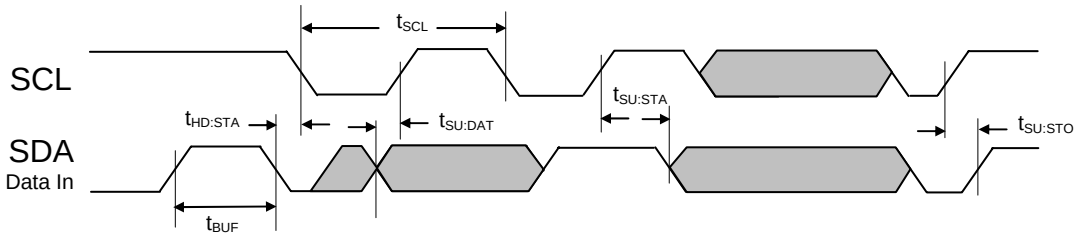
Notes:

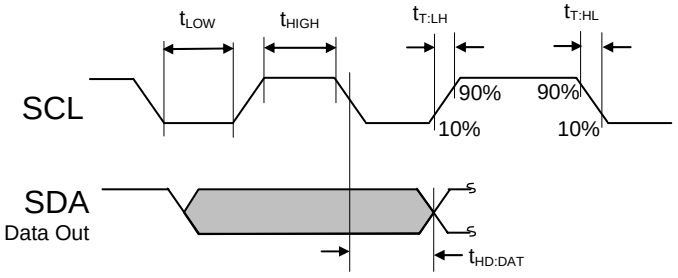
1. Absolute maximum ratings are limits beyond which operation may cause permanent damage to the device. These are stress ratings only; functional operation at or above these limits is not implied.
2. Human Body Model: 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Machine Model: 200pF capacitor discharged directly into each pin.
3. These specifications are guaranteed only for the test conditions listed.

4. This specification only indicates how often temperature information is updated to the Temperature Register. The aTS75 can be read at any time without interrupting the temperature conversion process.
5. Accuracy (expressed in °C) = Difference between the aTS75 output temperature and the measured temperature.

Serial Port Timing (T_A = 25 °C, V_{DD} = 5V unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SCL Clock Period	t_{SCL}		1.0		100	µs
SCL Clock Transition Time	$t_{T:LH}$, $t_{T:HL}$				300	ns
SCL Clock Low Period	t_{LOW}		0.470			µs
SCL Clock High Period	t_{HIGH}		0.400		50	µs
Bus free time between a Stop and a new Start Condition	t_{BUF}		1.0			µs
Data in Set-Up to SCL High	$t_{SU:DAT}$		100			ns
Data Out Stable after SCL Low	$t_{HD:DAT}$		0			ns
SCL Low Set-up to SDA Low (Repeated Start Condition)	$t_{SU:STA}$		100			ns
SCL High Hold after SDA Low (Start Condition)	$t_{HD:STA}$		100			ns
SDA High after SCL High (Stop Condition)	$t_{SU:STO}$		100			ns
Time in which aTS75 must be operational after a power-on reset	t_{POR}				500	ms





Pin Descriptions

Pin #	Name	Direction	Description
1	SDA	Input/Output	Serial Data—Open drain I/0-data pin for two-wire interface.
2	SCL	Input	Serial Clock—Clock for 2-wire serial interface.
3	O.S.	Output	Over-Limit Signal—Open drain thermostat output that indicates if the temperature has exceeded user-programmable limits
4	GND	Supply	Ground
5, 6,7	A0, A1, A2	Input	Address LSBs—User selectable address pins for the 3 lsbs of the serial interface address.
8	V_{DD}	Supply	Supply Voltage

Basic Operation

The aTS75 temperature sensing circuitry continuously produces an analog voltage that is proportional to the device temperature. At regular intervals the aTS75 converts the analog voltage to a two's complement digital value, which is placed into the temperature register.

The aTS75 has an SMBus compatible digital serial interface which allows the user to access the data in the temperature register at any time. In addition, the serial interface gives the user easy access to all other aTS75 registers to customize operation of the device.

The aTS75 temperature-to-digital conversion can have 9-, 10-, 11-, or 12-bit resolution as selected by the user, providing 0.5°C, 0.25°C, 0.125°C, and 0.0625°C temperature resolution, respectively. At power-up the default conversion resolution is 9-bits. The conversion resolution is controlled by the R0 and R1 bits in the Configuration Register.

Table 1 gives examples of the relationship between the output digital data and the external temperature. The 9-bit, 10-bit, 11-bit and 12-bit columns in Table 1 indicate the right-most bit in the output data stream that can contain temperature information for each conversion accuracy. Since the output digital data is in two's-complement format, the most significant bit of the temperature is the "sign" bit. If the sign bit is a zero, the temperature is positive and if the sign bit is a one, the temperature is negative.

The aTS75 has a Shutdown Mode that reduces the operating current of the aTS75 to 150nA. This mode is controlled by the SD bit in the configuration register.

Power Up Default Conditions

The ATS75 always powers up in the following default state:

- Thermostat mode: Comparator Mode
- O.S. polarity: active low
- Fault tolerance: 1 fault (i.e., F0=0 and F1=0 in the Configuration Register)
- T_{OS} = 80°C
- T_{HYST} = 75°C
- Register pointer: 00 (Temperature Register)
- Conversion resolution: 9 bits (i.e., R0=0 and R1=0 in the Configuration Register)

After power up these conditions can be reprogrammed via the serial interface. Refer to the Serial Data Bus Operation section to for aTS75 programming instructions.

Thermal Alarm Function

The aTS75 thermal alarm function provides user programmable thermostat capability and allows the aTS75 to function as a standalone thermostat without using the serial interface. The Over-Limit Signal (O.S.) output is the alarm output. This signal is an open drain output, and at power-up this pin is configured with active-low polarity.

Table 1. Relationship Between Temperature and Digital Output

Temperature	Digital Output							
	Sign Bit	Number of bits used by conversion resolution		9-bit	10-bit	11-bit	12-bit	Always zero
All Temperatures	12-Bit Resolution							0000
	11-Bit Resolution						0	0000
	10-Bit Resolution					0	0	0000
	9-Bit Resolution				0	0	0	0000
+125°C	0	111	1101	0	0	0	0	0000
+100.0625°C	0	110	0100	0	0	0	1	0000
+50.125°C	0	011	0010	0	0	1	0	0000
+12.25°C	0	000	1100	0	1	0	0	0000
0°C	0	000	0000	0	0	0	0	0000
-20.5°C	1	110	1011	1	0	0	0	0000
-33.25°C	1	101	1110	1	1	0	0	0000
-45.0625°C	1	101	0010	1	1	1	1	0000
-55°C	1	100	1001	0	0	0	0	0000

The O.S. polarity is controlled by the POL bit in the Configuration Register. The user-programmable upper trip-point temperature for the thermal alarm is stored in the T_{OS} Register, and the user-programmable hysteresis temperature (i.e., the lower trip point) is stored in the T_{HYST} Register.

The thermal alarm has two modes of operation: Comparator Mode and Interrupt Mode. At power-up the default is Comparator Mode. The alarm mode is controlled by the CMP/INTR bit in the Configuration Register.

Fault Tolerance

In either mode the alarm "fault tolerance" setting plays a role in determining when the O.S. output will be activated. Fault tolerance refers to the number of consecutive times an error condition must be detected before the user is notified. Higher fault tolerance settings can help eliminate false alarms caused by noise in the system. The alarm fault tolerance is controlled by bits F0 and F1 in the Configuration Register. These bits can be used to set the fault tolerance to 1, 2, 4 or 6 as shown in Table 4. At power-up, these bits both default to 0 (fault tolerance = 1).

Comparator Mode

In Comparator Mode, each time an temperature-to-digital(T-to-D) temperature conversion occurs, the new digital temperature is compared to the value stored in the T_{OS} and T_{HYST} Registers. If a fault tolerance number of consecutive temperature measurements are greater than the value stored in the T_{OS} Register, the O.S. output will be activated. For example, if bits F1 and F0 are equal to "10" (fault tolerance = 4), four consecutive temperature measurements must exceed T_{OS} to activate the O.S. output. Once the O.S output is active, it will remain active until the first time the measured temperature drops below the temperature stored in the T_{HYST} Register. The operation of the alarm in Comparator Mode with fault tolerance=2 is illustrated in Figure 1.

Interrupt Mode

In Interrupt Mode the O.S. output will first become active after a fault tolerance number of consecutive temperature measurements exceed the value stored in the T_{OS} Register (similar to Comparator Mode). Once O.S. is active, it can only be cleared by a user read from any of the aTS75 registers (Temperature, Configuration, T_{OS}, or T_{HYST}) or by putting the aTS75 into Shutdown Mode (i.e., by setting the shutdown bit in the Configuration Register to "1"). Once cleared, the O.S. output can only be activated again by a fault tolerance number of consecutive temperature measurements that are lower than the value stored in T_{HYST}. Again, once it is activated the O.S. output can only be deactivated by a user read or shutdown. Thus, in Interrupt Mode the activate/clear cycle for O.S. has the following pattern: temperature > T_{OS}, clear, temperature < T_{HYST}, clear, temperature > T_{OS}, clear, etc. The operation of the alarm in Interrupt Mode with fault tolerance=2 is also illustrated in Figure 1.

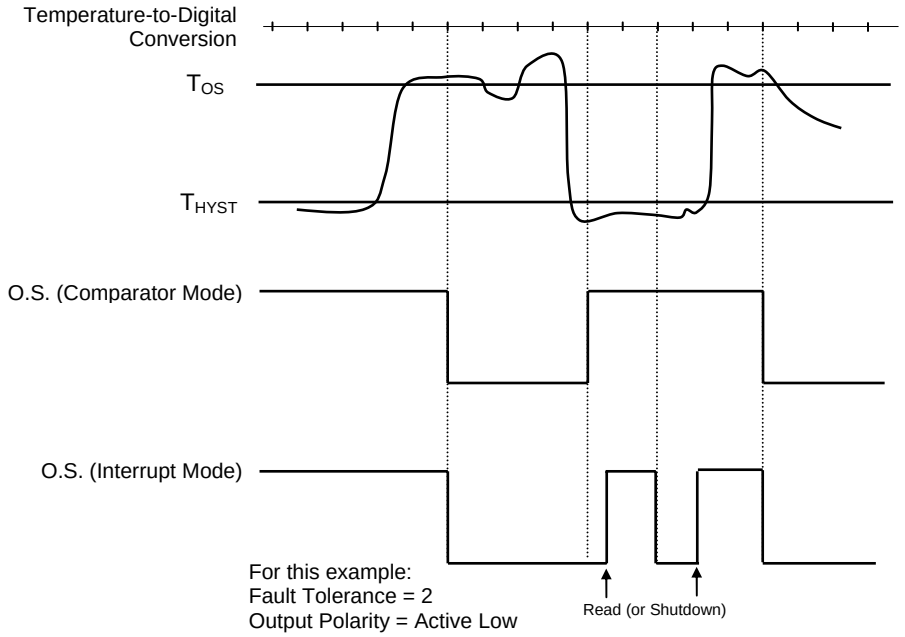


Figure 1. Thermal Alarm Operation in Comparator and Interrupt Modes

Registers

The ATS75 contains the following five registers:

1) Command Register
2) Temperature Register
3) Configuration Register
4) Over-Limit-Signal Temperature Register (T_{OS})
5) Hysteresis Temperature Register (T_{HYST})

All of these registers can be accessed by the user via the digital serial interface at anytime (see Serial Interface Operation for instructions). A detailed description of these registers and their functions is provided in the following paragraphs. A diagram of the register hierarchy is shown in Figure 2.

Command Register

The Command Register is a one-byte (8-bit) write-only register. The data stored in the Command Register indicates which of the other four registers (Temperature, Configuration, T_{HYST}, or T_{OS}) the user intends to read from or write to during an upcoming operation. In other words the Command Register "points" to the selected register as shown in Figure 2.

The Command Register is illustrated in Figure 3. The P1 and P0 bits of the Command Register determine which register is to be accessed as shown in Table 2. The six MSBs of the Command Register must always be zero. Writing a 1 into any of these bits will cause the current operation to be terminated.

The Command Register retains pointer information between operations. Therefore, this register only needs to be updated once for consecutive read operations from the same register. All bits in the Command Register default to zero at power-up.

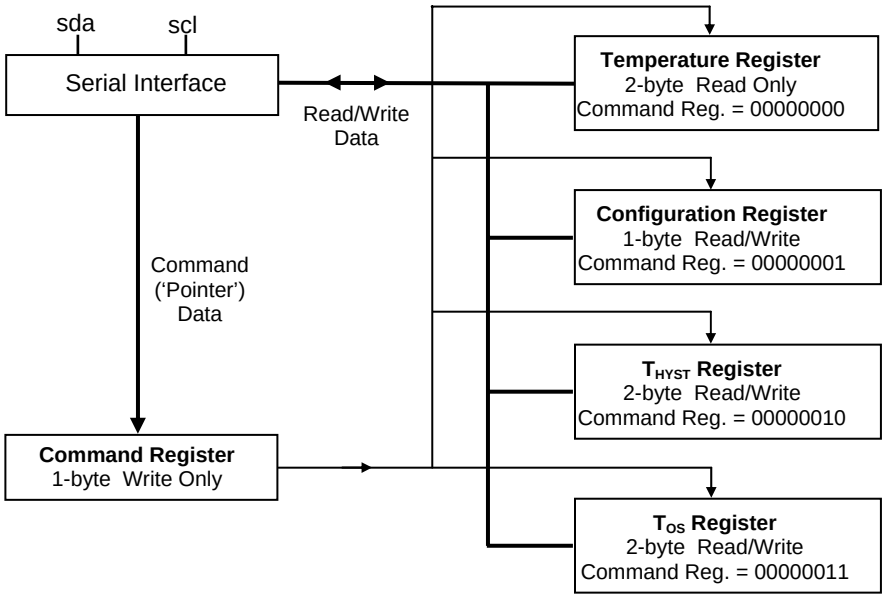


Figure 2. aTS75 Register Hierarchy

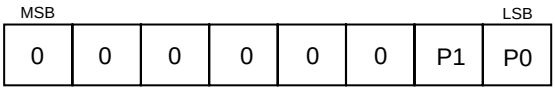


Figure 3. Command Register Format

Table 2. Register Assignments for Command Bits P1 and P2

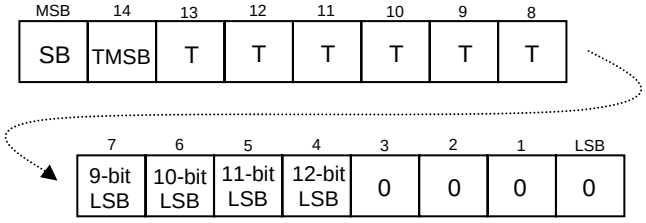
Register	P1	P0
Temperature Register	0	0
Configuration Register	0	1
T_{HYST} Register	1	0
T_{OS} Register	1	1

Temperature Register

The Temperature Register is a two-byte (16-bit) read-only register. Digital temperatures from the T-to-D converter are stored in the Temperature Register in two's complement format, and the contents of this register are updated at regular intervals—i.e., each time the T-to-D conversion is finished.

The user can read data from the Temperature Register at any time. When a T-to-D conversion is completed, the new data is loaded into a comparator buffer to evaluate fault conditions, and will update to the Temperature Register if a read cycle is not ongoing. The aTS75 is continuously evaluating fault conditions regardless of read or write activity on the bus. If a read is ongoing, the previous temperature will be read. The readable temperature will be updated upon the completion of the next T-to-D conversion that is not masked by a read cycle.

The Temperature Register is illustrated in Figure 4. Depending on the resolution of the T-to-D conversion, the 9, 10, 11 or 12 LSB's of the register will contain temperature data. All unused bits following the digital temperature will be zero. The MSB position of the Temperature Register always contains the sign bit for the digital temperature and bit 14 contains the temperature MSB. All bits in the Temperature Register default to zero at power-up.

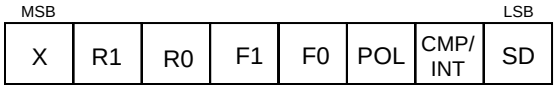


SB = Two's complement sign bit
TMSB = Temperature MSB
T = Temperature data
9-bit LSB = Temperature LSB for 9-bit conversions
10-bit LSB = Temperature LSB for 10-bit conversions
11-bit LSB = Temperature LSB for 11-bit conversions
12-bit LSB = Temperature LSB bit for 12-bit conversions

Figure 4. Temperature Register Format

Configuration Register

The Configuration Register is a one-byte (8-bit) read/write register (see Figure 5). This register allows the user to control the aTS75 Shutdown Mode as well as the following thermal alarm features: polarity, operating mode, and fault tolerance. The Configuration Register contains two bits that set the fault tolerance trip point. The fault tolerance trip point is the number of consecutive times the internal circuit reads the temperature and finds the temperature outside of the limits programmed. The programmed limits are defined by the T_{OS} Register for the upper limit, and by the T_{HYST} Register for the lower limit. Table 4 shows the relationship between F1 and F0 and the number of consecutive errors or "trips" needed to activate the alarm. The Configuration Register also contains two bits that set the T-to-D conversion resolution to 9-, 10-, 11-, or 12-bits. Table 3 shows the relationship between R1 and R0 and the conversion resolution. All bits in the Configuration Register default to zero at power-up.



R1 = Resolution bit 1. (See Table 3)
R0 = Resolution bit 0 . (See Table 3)
F1 = Fault tolerance bit 1. (See Table 4)
F0 = Fault tolerance bit 0 . (See Table 4)
POL = O.S. output polarity. 0 = active low, 1 = active high.
CMP/INT = Thermostat mode.
0 = Comparator Mode, 1 = Interrupt Mode.
SD = Shutdown. 0 = normal operation. 1 = Shutdown Mode

Figure 5. Configuration Register Format

Table 3. Conversion Resolution Settings

A-to-D Conversion Resolution	R1	R0
9 Bits	0	0
10 Bits	0	1
11 Bits	1	0
12 Bits	1	1

Table 4. Fault Tolerance Settings

Fault Tolerance	F1	F0
1	0	0
2	0	1
4	1	0
6	1	1

Over-Limit-Signal Temperature Register (T_{OS})

The T_{OS} Register is a two-byte (16-bit) read/write register that stores the user-programmable upper trip-point temperature for the thermal alarm in two's-complement format. At power-up this register defaults to 80°C (i.e., 0101 0000 0000 0000.

The format of the T_{OS} Register is identical to that of the Temperature Register (see Figure 6). The 4 LSBs of the T_{OS} Register are hardwired to zero, so data written to these register bits will be ignored. The MSB position of the T_{OS} Register contains the sign bit for the digital temperature and bit 14 contains the temperature MSB.

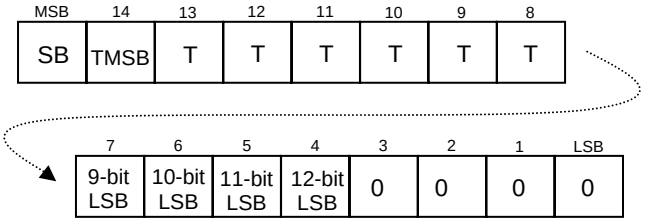
The resolution setting for the T-to-D conversion determines how many bits of the T_{OS} Register are used by the thermal alarm. For example, for 9-bit conversions the trip-point temperature is defined by the 9 MSBs of the T_{OS} Register, and all remaining bits are "don't cares".

Hysteresis Temperature Register (T_{HYST})

The T_{HYST} Register is a two-byte (16-bit) read/write register that stores the user programmable lower trip-point temperature for the thermal alarm in two's complement format. At power-up this register defaults to 75°C (i.e., 0100 1011 0000 0000).

The T_{HYST} Register is illustrated in Figure 6. The format of this register is the same as that of the Temperature Register. The 4 LSBs of the T_{HYST} Register are hardwired to zero, so data written to these bits is ignored.

The resolution setting for the T-to-D conversion determines how many bits of the T_{HYST} Register are used by the thermal alarm. For example, for 9-bit conversions the hysteresis temperature is defined by the 9 MSBs of the T_{HYST} Register, and all remaining bits are "don't cares".



SB = Two's complement sign bit
TMSB = Hysteresis temperature MSB
T = Temperature data
9-bit LSB = Hysteresis temperature LSB for 9-bit conversions
10-bit LSB = Hysteresis temperature LSB for 10-bit conversions
11-bit LSB = Hysteresis temperature LSB for 11-bit conversions
12-bit LSB = Hysteresis temperature LSB for 12-bit conversions

Figure 6. T_{HYST} Register and T_{OS} Register Format

Serial Data Bus Operation

General Operation

Writing to and reading from the aTS75 registers is accomplished via the SMBus-compatible two-wire serial interface. SMBus protocol requires that one device on the bus initiates and controls all read and write operations. This device is called the “master” device. The master device also generates the SCL signal which is the clock signal for all other devices on the bus. All other devices on the bus are called “slave” devices. The aTS75 is a slave device. Both the master and slave devices can send and receive data on the bus.

During SMBus operations, one data bit is transmitted per clock cycle. All SMBus operations follow a repeating nine clock-cycle pattern that consists of eight bits (one byte) of transmitted data followed by an acknowledge (ACK) or not acknowledge (NACK) from the receiving device. Note that there are no unused clock cycles during any operation—therefore there must be no breaks in the stream of data and ACKs/NACKs during data transfers. Conversely having too few clock cycles can lead to incorrect operation if an inadvertent 8-bit read from a 16-bit register occurs.

For most operations, SMBus protocol requires the SDA line to remain stable (unmoving) whenever SCL is high—i.e., transitions on the SDA line can only occur when SCL is low. The exceptions to this rule are when the master device issues a start or stop condition. Note that the slave device cannot issue a start or stop condition.

The following are definitions for some general SMBus terms:

Start Condition: This condition occurs when the SDA line transitions from high to low while SCL is high. The master device uses this condition to indicate that a data transfer is about to begin.

Stop Condition: This condition occurs when the SDA line transitions from low to high while SCL is high. The master device uses this condition to signal the end of a data transfer.

Acknowledge and **Not Acknowledge:** When data is transferred to the slave device sends an acknowledge(ACK) after receiving each byte of data. A master device sends an acknowledge(ACK) following only the first byte read from a 2-byte register. The receiving device sends an ACK by pulling SDA low for one clock. Following the last byte, a master device sends a "not acknowledge"(NACK) followed by a stop condition. A NACK is indicated by leaving SDA high during the clock after the last byte.

Slave Address

Each slave device on the bus has a unique 7-bit address so the master can identify which device is being read from or written to.

The aTS75 address is as follows:

1	0	0	1	A2	A1	A0

The four MSBs of the aTS75 address are hardwired to 1001. The three LSBs are user configurable by tying the A0, A1 and A2 pins to either V_{DD} or GND. This provides eight different aTS75 addresses, which allows up to eight aTS75s to be connected to the same bus.

Writing To and Reading From the aTS75

All read and write operations must begin with a start condition generated by the master device. After the start condition, the master device must immediately send a slave address (7 bits) followed by a read/write bit. If the slave address matches the address of the aTS75, the aTS75 sends an ACK after receiving the read/write bit by pulling the SDA line low for one clock. See Figure 8 – Figure 13 for timing diagrams for all aTS75 operations.

Setting the Pointer

For all operations the pointer stored in the Command Register must be pointing to the register (Temperature, Configuration, T_{OS} or T_{HYST}) that is going to be written to or read from. To change the pointer value in the Command Register, the read/write bit following the address must be 0. This indicates that the master will now write new information into the Command Register.

After the aTS75 sends an ACK in response to receiving the address and read/write bit, the master device must transmit an appropriate 8-bit pointer value as explained in the **Registers** section of this data sheet. The aTS75 will send an ACK after receiving the new pointer data.

The pointer set operation is illustrated in Figure 8. Anytime a pointer set is performed, it must be immediately followed by a read or write operation. Note that the 6 MSBs of the pointer value must be zero. If the 6 MSBs are not zero, the aTS75 will not send an ACK and will internally terminate the operation. Also recall that the Command Register retains the current pointer value between operations. Therefore, once a register is being pointed to, subsequent read operations do not require a pointer set cycle.

Reading

If the pointer is already pointing to the desired register, the master can read from that register by setting the read/write bit (following the slave address) to a 1. After sending an ACK, the aTS75 will begin transmitting data during the following clock cycle. If the Configuration Register is being read, the aTS75 will transmit one byte of data (see Figure 10). The master device should respond with a NACK followed by a stop condition. If the Temperature, T_{OS} or T_{HYST} Register is being read, the aTS75 will transmit two bytes of data (see Figure 9). The master must respond to the first byte of data with an ACK and to the second byte of data with a NACK followed by a stop condition.

To read from a register other than the one currently being pointed to by the Command Register, a pointer set to the desired register must be done as described previously. Immediately following the pointer set, the master must perform a repeat start condition (see Figures 8 and 12) which indicates to the aTS75 that a read is about to occur. It is important to note that if the repeat start condition does not occur, the aTS75 will assume that a write is taking place, and the selected register will be overwritten by the upcoming data on the data bus. After the start condition, the master must again send the device address and read/write bit. This time the read/write bit must be set to 1 to indicate a read. The rest of the read cycle is the same as described in the previous paragraph for reading from a preset pointer location.

Writing

All writes must be preceeded by a pointer set as described previously, even if the pointer is already pointing to the desired register.

Immediately following the pointer set, the master must begin transmitting the data to be written. If the master is writing to the Configuration Register, only one byte of data must be sent (see Figure 13). If the T_{OS} or T_{HYST} Register is being written to, the master must send two bytes of data (see Figure 11). After transmitting each byte of data, the master must release the SDA line for one clock to allow the aTS75 to acknowledge receiving the byte. The write operation should be terminated by a stop condition from the master.

Inadvertent 8-Bit Read from a 16-Bit Register: A Caution

An inadvertent 8-bit read from a 16-bit register, with the D7 bit low, can cause the aTS75 to pause in a state where the SDA line is pulled low by the output data and is incapable of receiving either a stop or a start condition from the master. The only way to remove the aTS75 from this state is to continue clocking for 9 cycles until SDA goes high, at which time issuing a stop condition will reset the aTS75. This sequence can be seen in Figure 7 below.

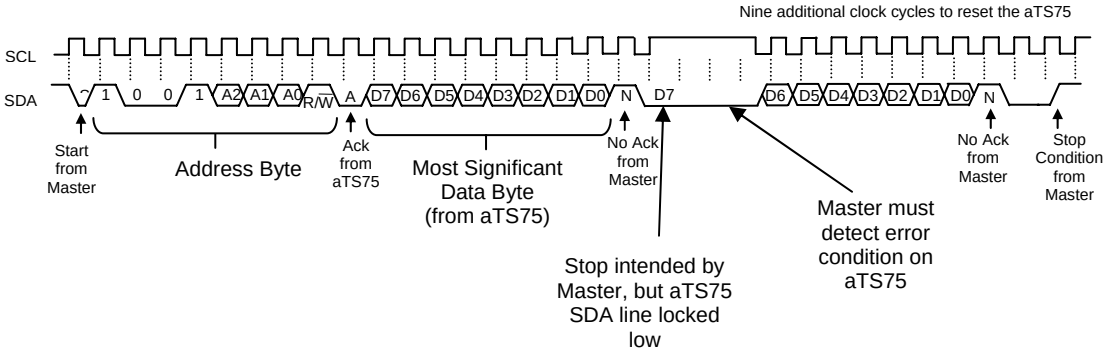


Figure 7. Inadvertent 8-Bit Read from 16-Bit Register where D7 = 0 and Forces Output Low

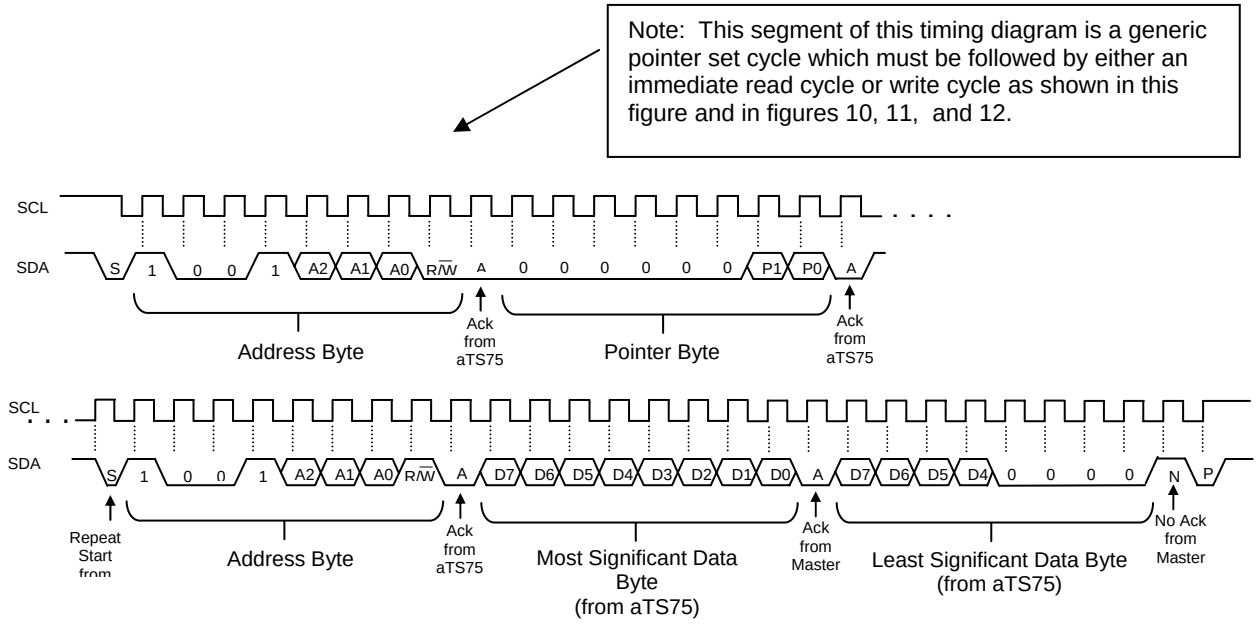


Figure 8. Pointer set followed by immediate read from a 2-byte register (Temperature, T_{OS}, or T_{HYST} Register)

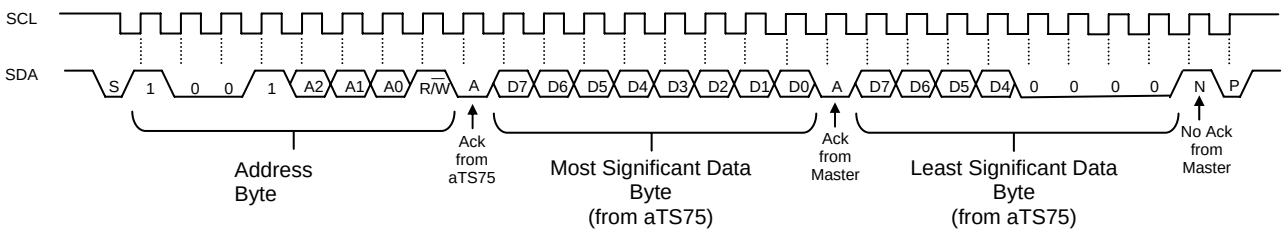


Figure 9. Two-byte read from preset pointer location (Temperature, T_{OS}, or T_{HYST} Register)

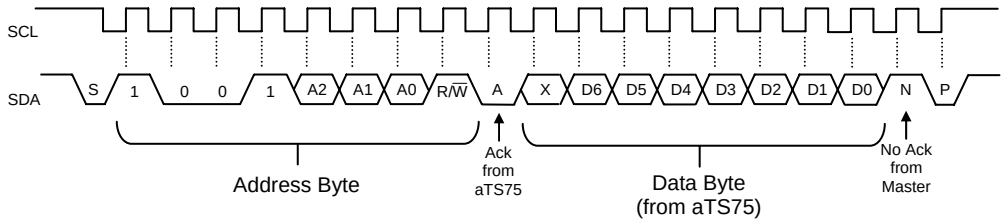


Figure 10 . One-byte read from Configuration Register with preset pointer

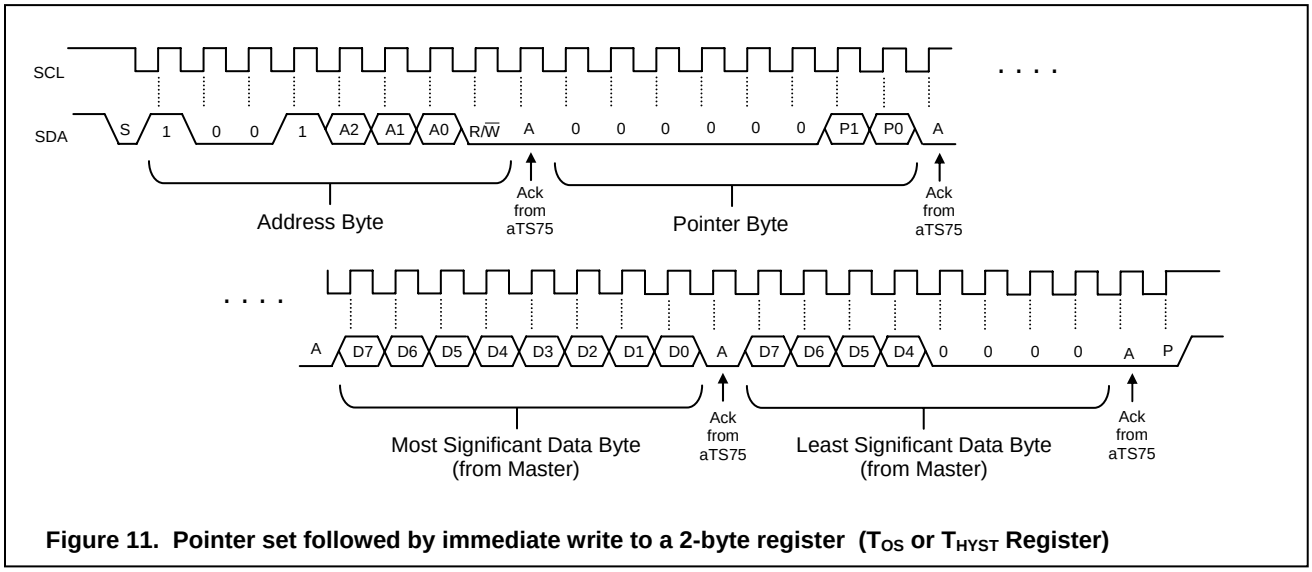


Figure 11. Pointer set followed by immediate write to a 2-byte register (T_{OS} or T_{HYST} Register)

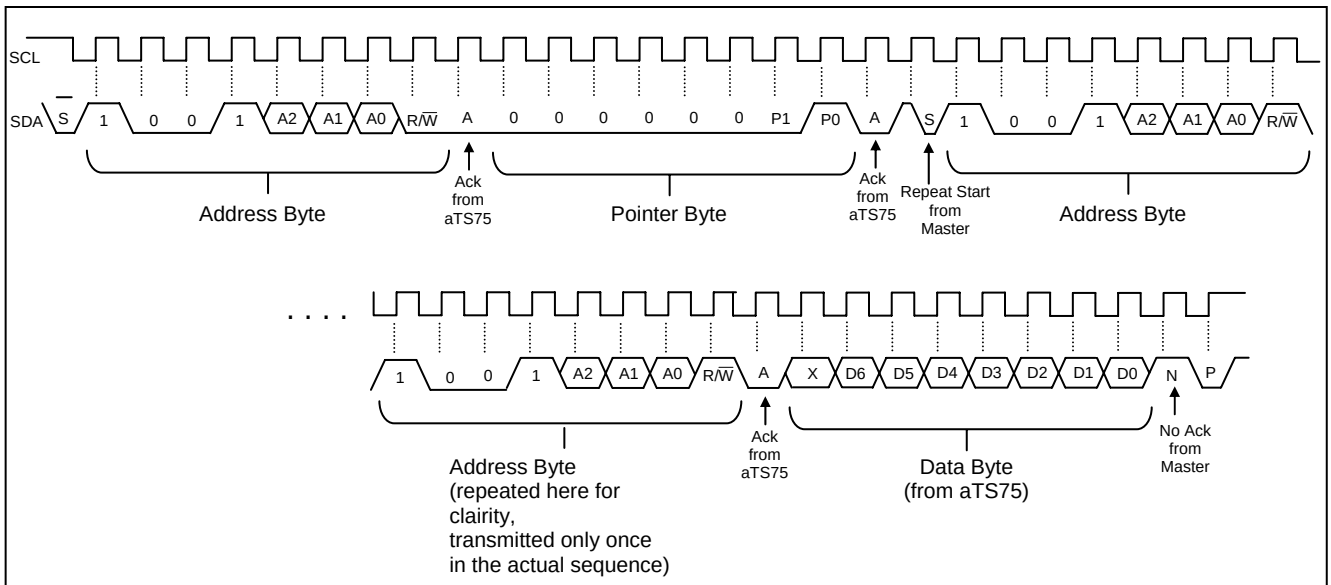


Figure 12. Pointer set followed by immediate read from Configuration Register

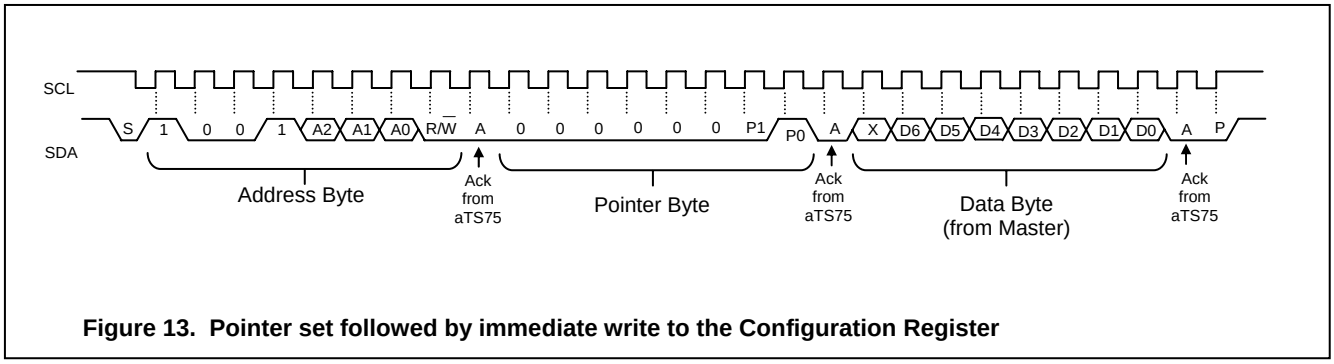
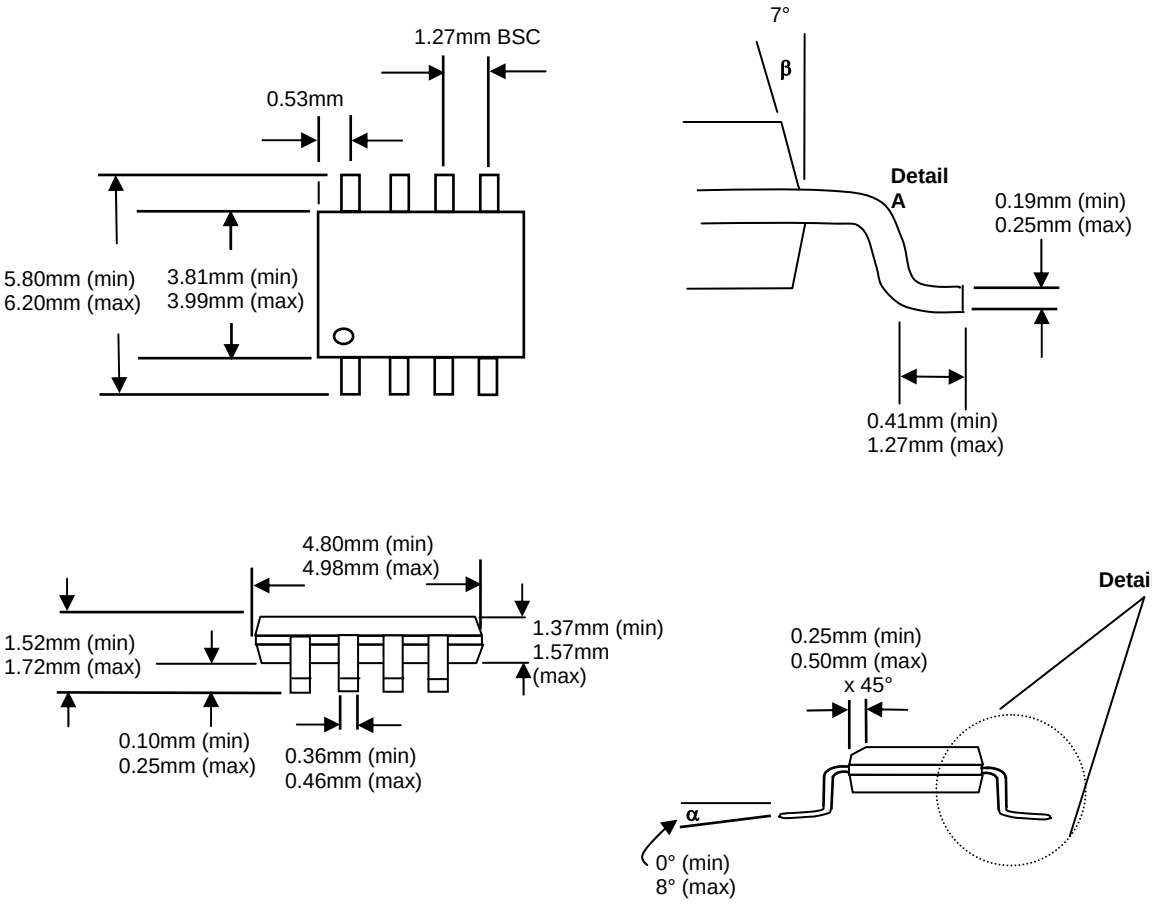
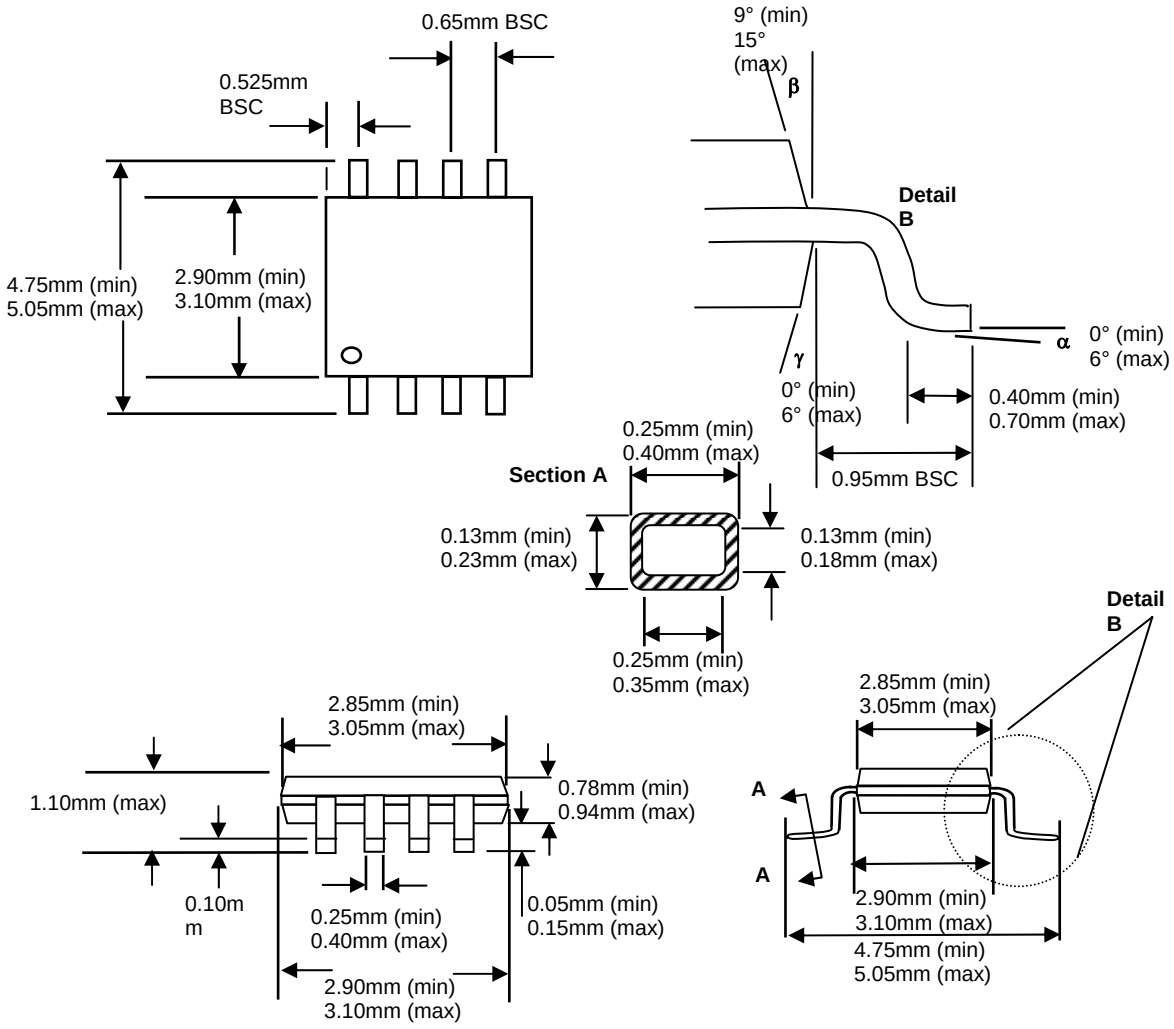


Figure 13. Pointer set followed by immediate write to the Configuration Register

D8 Package – 8-Lead SOIC Package Dimensions



M8 Package – 8-Lead MSOP Package Dimensions



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Andigilog, Inc.
8380 S. Kyrene Rd., Suite 101
Tempe, Arizona 85284
Tel: (480) 940-6200
Fax: (480) 940-4255

Notes:

Andigilog, Inc.
8380 S. Kyrene Rd., Suite 101
Tempe, Arizona 85284
Tel: (480) 940-6200
Fax: (480) 940-4255