Burr-Brown Products
from Texas Instruments

PCM1742



www.ti.com

24-Bit, 192kHz Sampling Enhanced Multilevel, Delta-Sigma, Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 24-BIT RESOLUTION
- ANALOG PERFORMANCE (V_{CC} = +5V):
  Dynamic Range: 106dB typ (PCM1742KE)
  100dB typ (PCM1742E)
  SNR: 106dB typ (PCM1742KE)
  100dB typ (PCM1742E)
  THD+N: 0.002% typ (PCM1742KE)
  0.003% typ (PCM1742E)
  Full-Scale Output: 3.1Vp-p typ
- 4x/8x OVERSAMPLING DIGITAL FILTER:
  Stopband Attenuation: –55dB
  Passband Ripple: ±0.03dB
- SAMPLING FREQUENCY: 5kHz to 200kHz
- SYSTEM CLOCK: 128, 192, 256, 384, 512, 768f_S with Auto Detect
- ACCEPTS 16-, 18-, 20-, AND 24-BIT AUDIO DATA
- DATA FORMATS: Standard, I²S, and Left-Justified
- USER-PROGRAMMABLE MODE CONTROLS:
  Digital Attenuation: 0dB to –63dB, 0.5dB/Step
  Digital De-Emphasis
  Digital Filter Roll-Off: Sharp or Slow
  Soft Mute
  Zero Flags for Each Output
- DUAL-SUPPLY OPERATION:
  +5V Analog, +3.3V Digital
- 5V TOLERANT DIGITAL INPUTS
- SMALL SSOP-16 PACKAGE
- SAME PACKAGE SIZE AS SOP-8

APPLICATIONS

- AV RECEIVERS
- DVD MOVIE PLAYERS
- DVD ADD-ON CARDS FOR HIGH-END PCs
- DVD AUDIO PLAYERS
- HDTV RECEIVERS
- CAR AUDIO SYSTEMS
- OTHER APPLICATIONS REQUIRING 24-BIT AUDIO

DESCRIPTION

The PCM1742 is a CMOS, monolithic, integrated circuit which includes stereo Digital-to-Analog Converters (DACs) and support circuitry in a small SSOP-16 package. The data converters utilize Texas Instrument's enhanced multilevel delta-sigma architecture that employs fourth-order noise shaping and 8-level amplitude quantization to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1742 accepts industry standard audio data formats with 16- to 24-bit data, providing easy interfacing to audio DSP and decoder chips. Sampling rates up to 200kHz are supported. A full set of user-programmable functions are accessible through a 3-wire serial control port that supports register write functions.

TEXAS INSTRUMENTS

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SBAS176

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SPECIFICATIONS

All specifications at T_A = +25°C, V_{CC} = 5.0V, V_{DD} = 3.3V, f_S = 44.1kHz, system clock = 384f_S, and 24-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1742E PCM1742KE MIN	TYP	MAX	UNITS
RESOLUTION			24		Bits
DATA FORMAT					
Audio Data Interface Formats			Standard, I²S, Left-Justified		
Audio Data Bit Length			16-, 18-, 20-, 24-Bits Selectable		
Audio Data Format			MSB-First, Binary Two's Complement		
Sampling Frequency (f_S)		5		100	kHz
System Clock Frequency			256, 384, 512, 768f_S		
DIGITAL INPUT/OUTPUT					
Logic Family			TTL-Compatible		
Input Logic Level					
V_{IH}		2.0			VDC
V_{IL}				0.8	VDC
Input Logic Current					
I_{IH}(1)	$V_{IN} = V_{DD}$			10	µA
I_{IL}(1)	V_{IN} = 0V			–10	µA
I_{IH}(2)	$V_{IN} = V_{DD}$		65	100	µA
I_{IL}(2)	V_{IN} = 0V			–10	µA
Output Logic Level					
V_{OH}(3)	I_{OH} = –2mA	2.4			VDC
V_{OL}(3)	I_{OL} = +2mA			1.0	VDC
DYNAMIC PERFORMANCE(4) (5)					
PCM1742E					
THD+N at V_{OUT} = 0dB	f_S = 44.1kHz		0.003	0.008	%
	f_S = 96kHz		0.004		%
	f_S = 192kHz		0.005		%
THD+N at V_{OUT} = –60dB	f_S = 44.1kHz		1.2		%
	f_S = 96kHz		1.6		%
	f_S = 192kHz		1.8		%
Dynamic Range	EIAJ, A-Weighted, f_S = 44.1kHz	94	100		dB
	A-Weighted, f_S = 96kHz		98		dB
	A-Weighted, f_S = 192kHz		96		dB
Signal-to-Noise Ratio	EIAJ, A-Weighted, f_S = 44.1kHz	94	100		dB
	A-Weighted, f_S = 96kHz		98		dB
	A-Weighted, f_S = 192kHz		96		dB
Channel Separation	f_S = 44.1kHz	91	98		dB
	f_S = 96kHz		96		dB
	f_S = 192kHz		94		dB
Level Linearity Error	V_{OUT} = –90dB		±0.5		dB
PCM1742KE					
THD+N at V_{OUT} = 0dB	f_S = 44.1kHz		0.002	0.006	%
	f_S = 96kHz		0.003		%
	fS = 192kHz		0.004		%
THD+N at V_{OUT} = –60dB	f_S = 44.1kHz		0.65		%
	f_S = 96kHz		0.8		%
	f_S = 192kHz		0.95		%
Dynamic Range	EIAJ, A-Weighted, f_S = 44.1kHz	100	106		dB
	A-Weighted, f_S = 96kHz		104		dB
	A-Weighted, f_S = 192kHz		102		dB
Signal-to-Noise Ratio	EIAJ, A-Weighted, f_S = 44.1kHz	100	106		dB
	A-Weighted, f_S = 96kHz		104		dB
	A-Weighted, f_S = 192kHz		102		dB
Channel Separation	f_S = 44.1kHz	97	103		dB
	f_S = 96kHz		101		dB
	f_S = 192kHz		100		dB
Level Linearity Error	V_{OUT} = –90dB		±0.5		dB
DC ACCURACY					
Gain Error			±1.0	±6	% of FSR
Gain Mismatch, Channel-to-Channel			±1.0	±3	% of FSR
Bipolar Zero Error	V_{OUT} = 0.5 V_{CC} at Bipolar Zero		±30	±60	mV
ANALOG OUTPUT					
Output Voltage	Full Scale (0dB)		62% of V_{CC}		Vp-p
Center Voltage			50% V_{CC}		VDC
Load Impedance	AC Load	5			kΩ
DIGITAL FILTER PERFORMANCE					
Filter Characteristics 1, Sharp Roll-Off					
Passband	±0.03dB			0.454f_S	
Passband	–3dB			0.487f_S	
Stopband		0.546f_S			dB
Passband Ripple				±0.03	dB
Stopband Attenuation	Stopband = 0.546f_S	–50			dB
Stopband Attenuation	Stopband = 0.567f_S	–55			

SPECIFICATIONS (Cont.)

All specifications at T_A = +25°C, V_{CC} = 5.0V, V_{DD} = 3.3V, system clock = 384f_S (f_S = 44.1kHz), and 24-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1742E PCM1742KE MIN	TYP	MAX	UNITS
DIGITAL FILTER PERFORMANCE (Cont.)					
Filter Characteristics 2, Slow Roll-Off					
Passband	±0.5dB			0.198f_S	
Passband	–3dB			0.390f_S	
Stopband		0.884f_S			
Passband Ripple				±0.5	dB
Stopband Attenuation	Stopband = 0.884f_S	–40			dB
Delay Time			20/f_S		sec
De-Emphasis Error			±0.1		dB
ANALOG FILTER PERFORMANCE					
Frequency Response	f = 20kHz		–0.03		dB
	f = 44kHz		–0.20		dB
POWER SUPPLY REQUIREMENTS(4)					
Voltage Range, V_{DD}		+3.0	+3.3	+3.6	VDC
V_{CC}		+4.5	+5.0	+5.5	VDC
Supply Current, I_{DD}	f_S = 44.1kHz		6.0	10	mA
	f_S = 96kHz		13		mA
	f_S = 192kHz		16		mA
I_{CC}	f_S = 44.1kHz		8.5	13	mA
	f_S = 96kHz		9.0		mA
	f_S = 192kHz		9.0		mA
Power Dissipation	f_S = 44.1kHz		62	98	mW
	f_S = 96kHz		88		mW
	f_S = 192kHz		98		mW
TEMPERATURE RANGE					
Operation Temperature		–25		+85	°C
Thermal Resistance θ_{JA}	SSOP-16		115		°C/W

NOTES: (1) Pins 1, 2, 3, 16 (SCK, BCK, LRCK, DATA). (2) Pins 13-15 (MD, MC, ML). (3) Pins 11, 12 (ZEROR, ZEROL). (4) Analog performance specifications are tested with a Shibasoku #725 THD Meter with 400Hz HPF on, 30kHz LPF on, and an average mode with 20kHz bandwidth limiting. The load connected to the analog output is 5kΩ or larger, via capacitive coupling. (5) Conditions in 192kHz operation are: system clock = 128f_S and oversampling rate = 64f_S of Register 18.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, V_{DD}	+4.0V
V_{CC}	+6.5V
Ground Voltage Differences	±0.1V
Digital Input Voltage	–0.3V to (6.5V + 0.3V)
Input Current (except power supply)	±10mA
Ambient Temperature Under Bias	–40°C to +125°C
Storage Temperature	–55°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 5s)	+260°C
Package Temperature (IR reflow, 10s)	+235°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

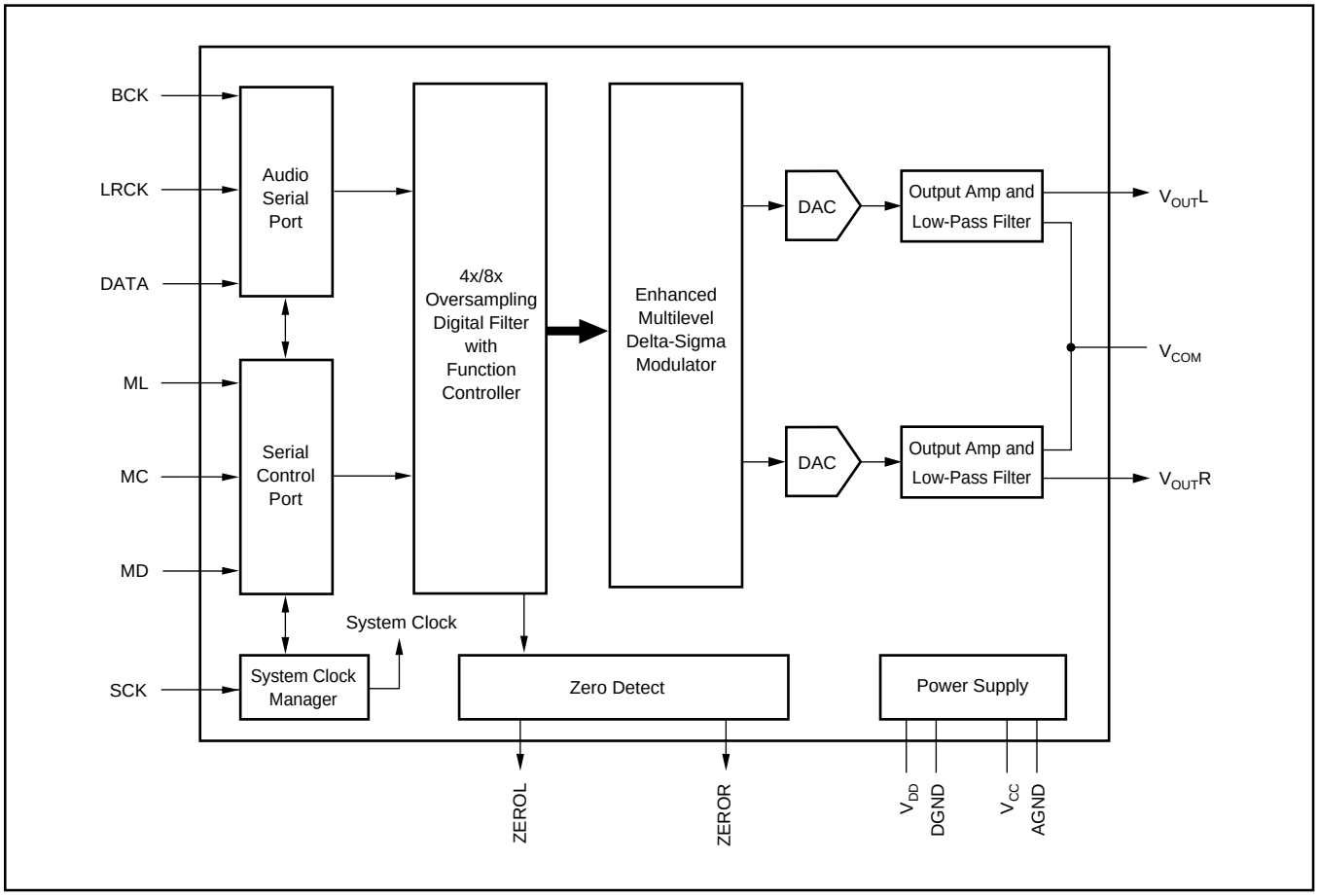
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
PCM1742E	SSOP-16	322	–25°C to +85°C	PCM1742E	PCM1742E	Rails
"	"	"	"	"	PCM1742E/2K	Tape and Reel
PCM1742KE	SSOP-16	322	–25°C to +85°C	PCM1742KE	PCM1742KE	Rails
"	"	"	"	"	PCM1742KE/2K	Tape and Reel

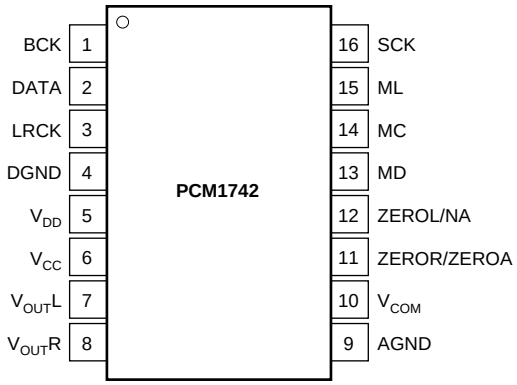
NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "PCM1742E/2K" will yield a single 2000-piece Tape and Reel.

BLOCK DIAGRAM



PIN CONFIGURATION

TOP VIEW **SSOP**



PIN ASSIGNMENTS

PIN	NAME	TYPE	FUNCTION
1	BCK	IN	Audio Data Bit Clock Input.(1)
2	DATA	IN	Audio Data Digital Input.(1)
3	LRCK	IN	L-Channel and R-Channel Audio Data Latch Enable Input.(1)
4	DGND	–	Digital Ground
5	V_{DD}	–	Digital Power Supply, +3.3V
6	V_{CC}	–	Analog Power Supply, +5V
7	$V_{OUT}L$	OUT	Analog Output for L-Channel.
8	$V_{OUT}R$	OUT	Analog Output for R-Channel.
9	AGND	–	Analog Ground
10	V_{COM}	–	Common Voltage Decoupling.
11	ZEROR/ ZEROA	OUT	Zero Flag Output for R-Channel/Zero Flag Output for L/R-Channel.
12	ZEROL/NA	OUT	Zero Flag Output for L-Channel/No Assign.
13	MD	IN	Mode Control Data Input.(2)
14	MC	IN	Mode Control Clock Input.(2)
15	ML	IN	Mode Control Latch Input.(2)
16	SCK	IN	System Clock Input.

NOTES: (1) Schmitt-trigger input, 5V tolerant. (2) Schmitt-trigger with internal pull-down, 5V tolerant.

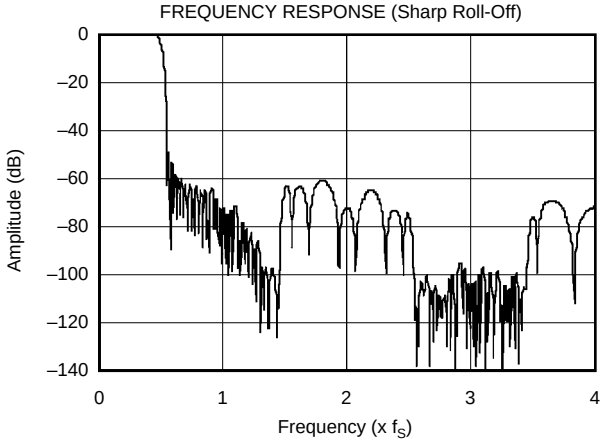
TYPICAL PERFORMANCE CURVES

All specifications at T_A = +25°C, V_{CC} = 5.0V, V_{DD} = 3.3V, system clock = 384f_S (f_S = 44.1kHz), and 24-bit input data, unless otherwise noted.

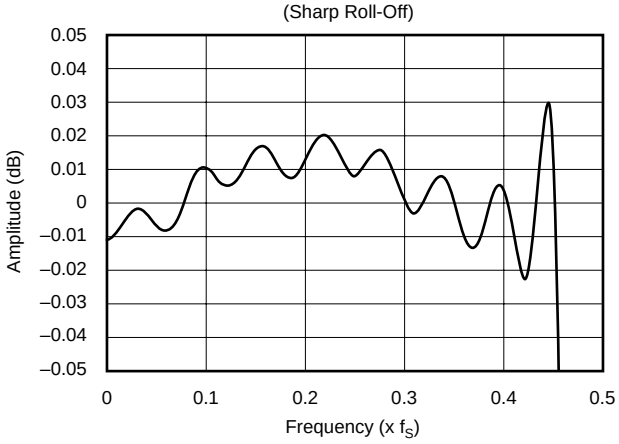
DIGITAL FILTER

Digital Filter (De-Emphasis Off)

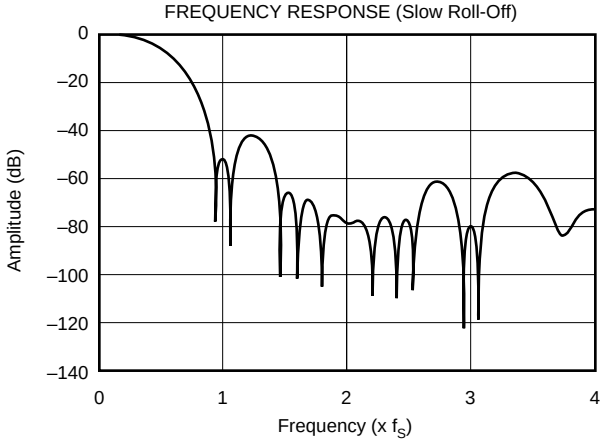
FREQUENCY RESPONSE (Sharp Roll-Off)



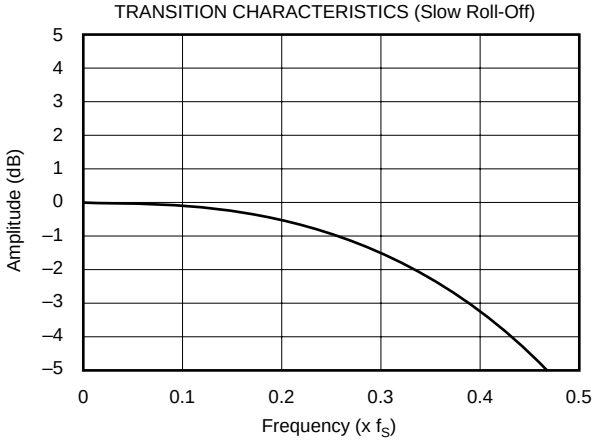
FREQUENCY RESPONSE PASSBAND
(Sharp Roll-Off)



FREQUENCY RESPONSE (Slow Roll-Off)

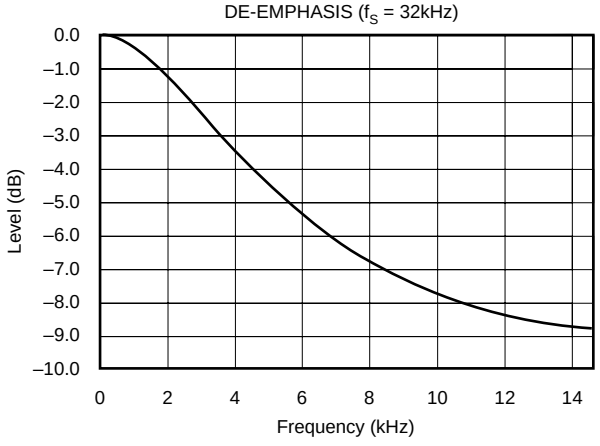


TRANSITION CHARACTERISTICS (Slow Roll-Off)

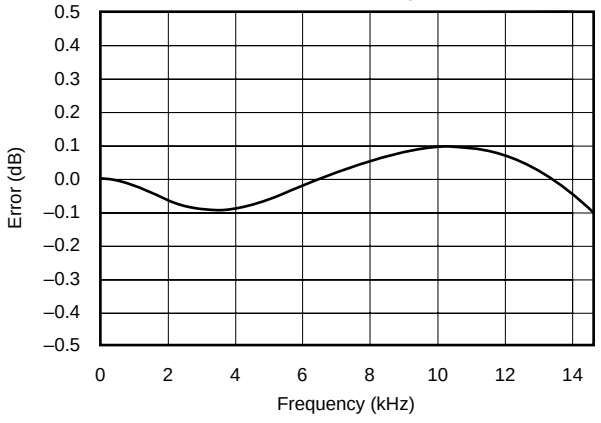


De-Emphasis

DE-EMPHASIS (f_S = 32kHz)



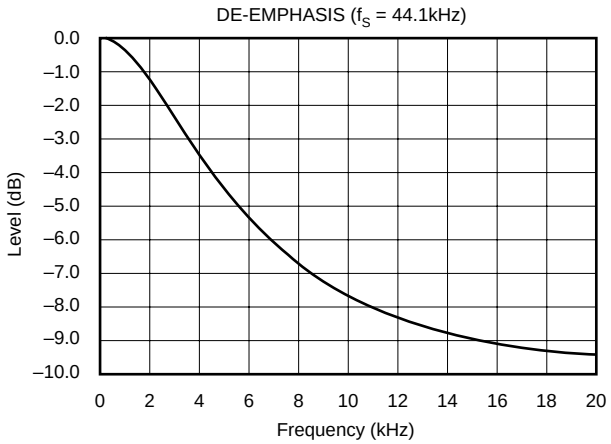
DE-EMPHASIS ERROR (f_S = 32kHz)

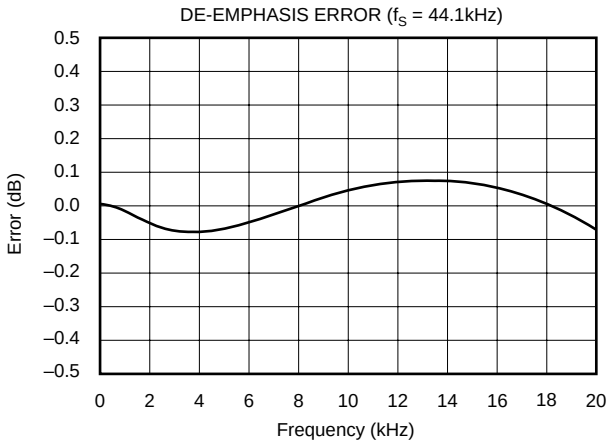


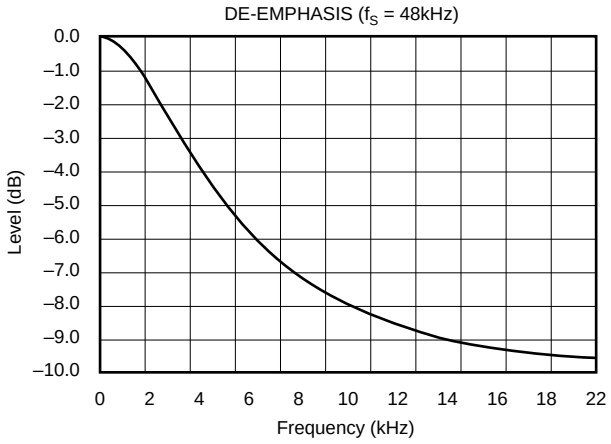
TYPICAL PERFORMANCE CURVES (Cont.)

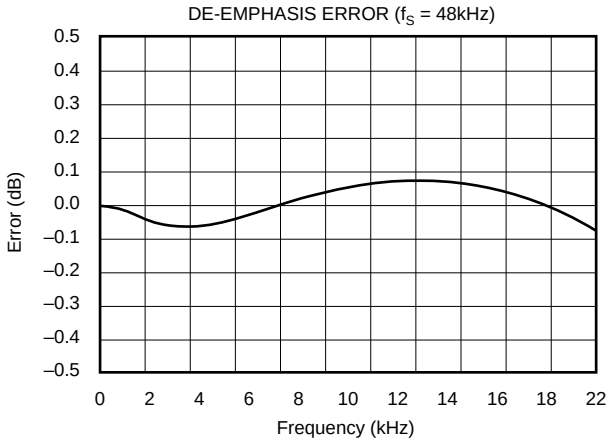
All specifications at T_A = +25°C, V_{CC} = 5.0V, V_{DD} = 3.3V, system clock = 384f_S (f_S = 44.1kHz), and 24-bit input data, unless otherwise noted.

De-Emphasis (Cont.)





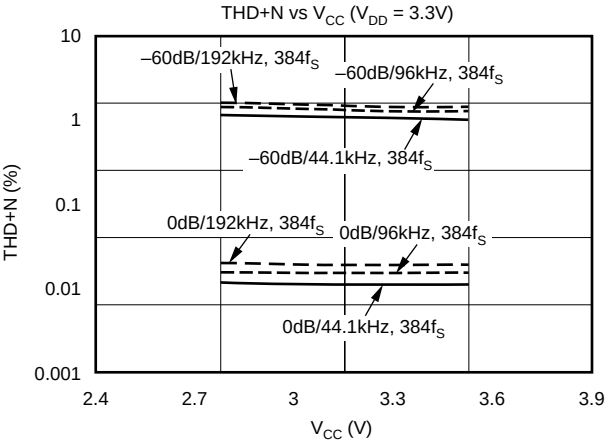


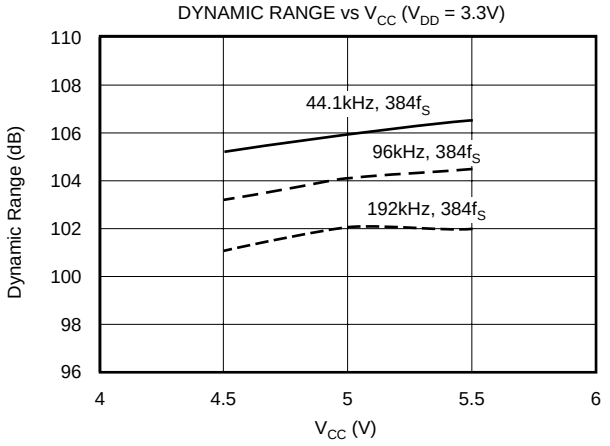


ANALOG DYNAMIC PERFORMANCE

All specifications at T_A = +25°C, V_{CC} = 5.0V, V_{DD} = 3.3V, and 24-bit input data, unless otherwise noted. Conditions in 192kHz operation are: system clock = 128f_S and oversampling rate = 64f_S of Register 18.

Supply-Voltage Characteristics

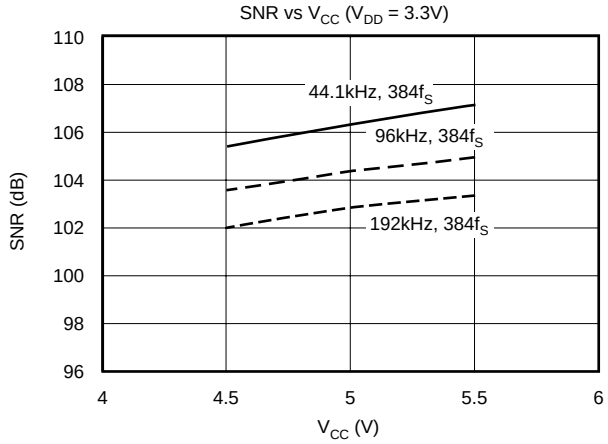


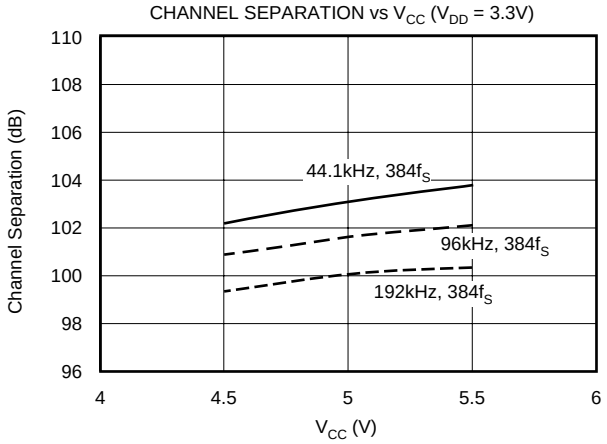


TYPICAL PERFORMANCE CURVES (Cont.)

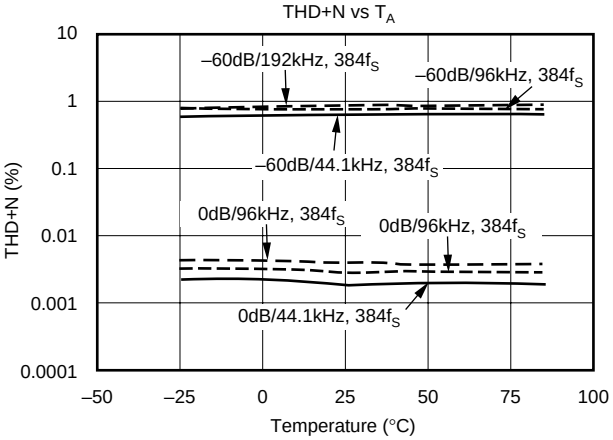
All specifications at T_A = +25°C, V_{CC} = 5.0V, V_{DD} = 3.3V, and 24-bit input data, unless otherwise noted. Conditions in 192kHz operation are: system clock = 128f_S and oversampling rate = 64f_S of Register 18.

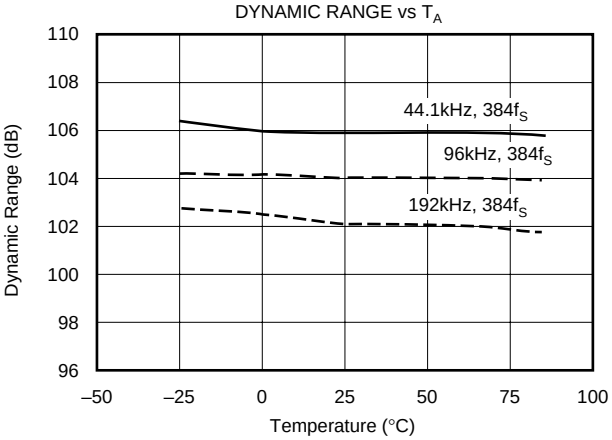
Supply-Voltage Characteristics (Cont.)

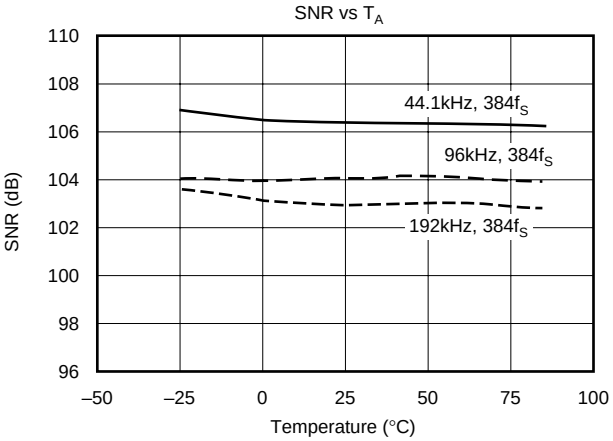


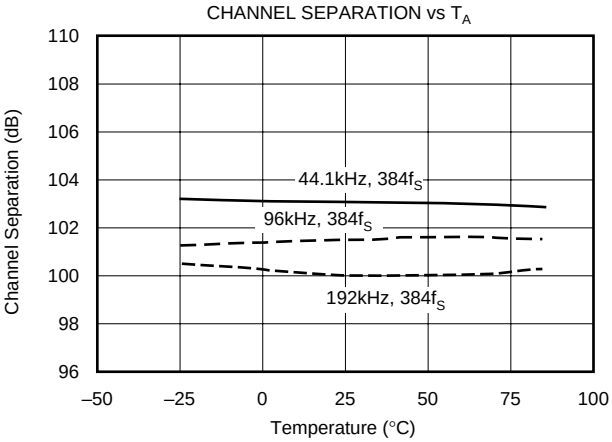


Temperature Characteristics









SYSTEM CLOCK AND RESET FUNCTIONS

SYSTEM CLOCK INPUT

The PCM1742 requires a system clock for operating the digital interpolation filters and multilevel delta-sigma modulators. The system clock is applied at the SCK input (pin 16). Table I shows examples of system clock frequencies for common audio sampling rates.

Figure 1 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. The PLL1700 multi-clock generator from Texas Instruments is an excellent choice for providing the PCM1742 system clock.

POWER-ON RESET FUNCTIONS

The PCM1742 includes a power-on reset function, as shown in Figure 2. With the system clock active, and $V_{DD} > 2.0V$ (typical 1.6V to 2.4V), the power-on reset function will be enabled. The initialization sequence requires 1024 system clocks from the time $V_{DD} > 2.0V$. After the initialization period, the PCM1742 will be set to its reset default state, as described in the Mode Control Register section of this data sheet.

During the reset period (1024 system clocks), the analog outputs are forced to the bipolar zero level, or $V_{CC}/2$. After the reset period, the internal register is initialized in the next $1/f_S$ period and, if SCK, BCK, and LRCK are provided continuously, the PCM1742 provides proper analog output with unit group delay against the input data.

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)					
	128f_S	192f_S	256f_S	384f_S	512f_S	768f_S
8kHz	—	—	2.0480	3.0720	4.0960	6.1440
16kHz	—	—	4.0960	6.1440	8.1920	12.2880
32kHz	—	—	8.1920	12.2880	16.3840	24.5760
44.1kHz	—	—	11.2896	16.9344	22.5792	33.8688
48kHz	—	—	12.2880	18.4320	24.5760	36.8640
88.2kHz	—	—	22.5792	33.8688	45.1584	See Note (1)
96kHz	—	—	24.5760	36.8640	49.1520	See Note (1)
192kHz	24.5760	36.8640	See Note (1)	See Note (1)	See Note (1)	See Note (1)

NOTE: (1) This system clock is not supported for the given sampling frequency.

TABLE I. System Clock Rates for Common Audio Sampling Frequencies.

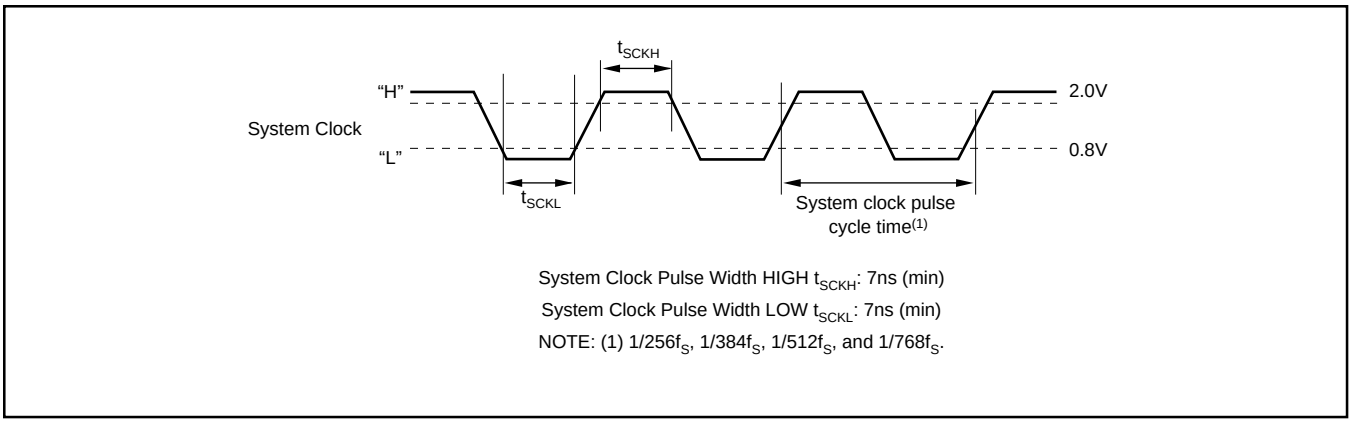


FIGURE 1. System Clock Input Timing.

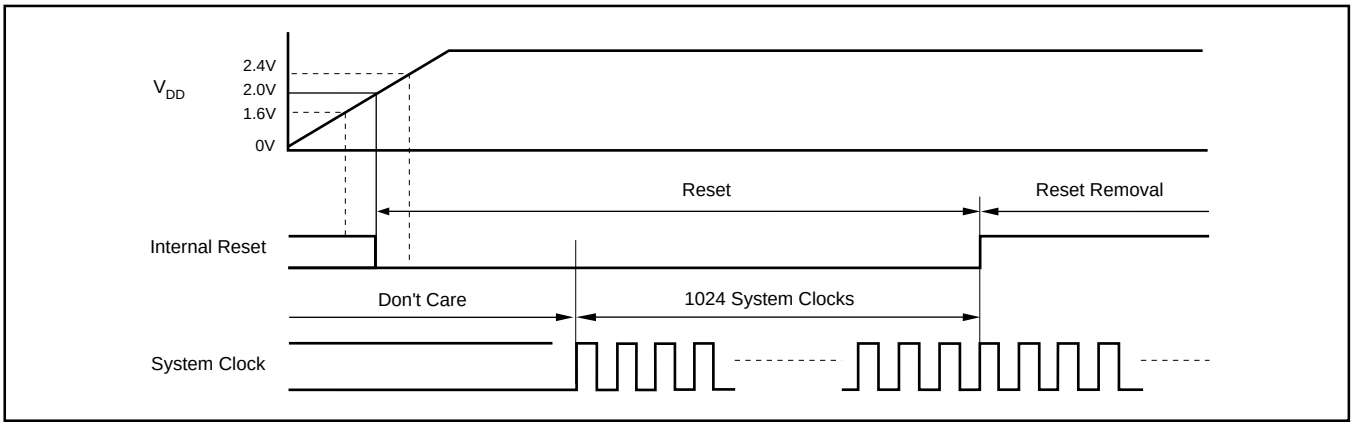


FIGURE 2. Power-On Reset Timing.

AUDIO SERIAL INTERFACE

The audio serial interface for the PCM1742 is comprised of a 3-wire synchronous serial port. It includes LRCK (pin 3), BCK (pin 1), and DATA (pin 2). BCK is the serial audio bit clock, and is used to clock the serial data present on DATA into the audio interface's serial shift register. Serial data is clocked into the PCM1742 on the rising edge of BCK. LRCK is the serial audio left/right word clock used to latch serial data into the serial audio interface's internal registers.

Both LRCK and BCK should be synchronous to the system clock. Ideally, it is recommended that LRCK and BCK be derived from the system clock input, SCK. LRCK is operated at the sampling frequency, f_S. BCK may be operated at 32, 48, or 64 times the sampling frequency (I^2S format except BCK = $32f_S$). Internal operation of the PCM1742 is synchronized with LRCK. Accordingly, it is held when the sampling rate clock of LRCK is changed or SCK and/or BCK is broken at least for one clock cycle. If SCK, BCK, and LRCK are provided continuously after this hold condition, the internal operation will be resynchronized automatically, less than $3/f_S$ period. In this resynchronize period, and following $3/f_S$, analog output is forced to the bipolar zero level, or $V_{CC}/2$. External resetting is not required.

AUDIO DATA FORMATS AND TIMING

The PCM1742 supports industry-standard audio data formats, including Standard, I^2S, and Left-Justified, as shown in Figure 3. Data formats are selected using the format bits, FMT[2:0], in Control Register 20. The default data format is 24-bit left justified. All formats require Binary Two's Complement, MSB-first audio data. See Figure 4 for a detailed timing diagram of the serial audio interface.

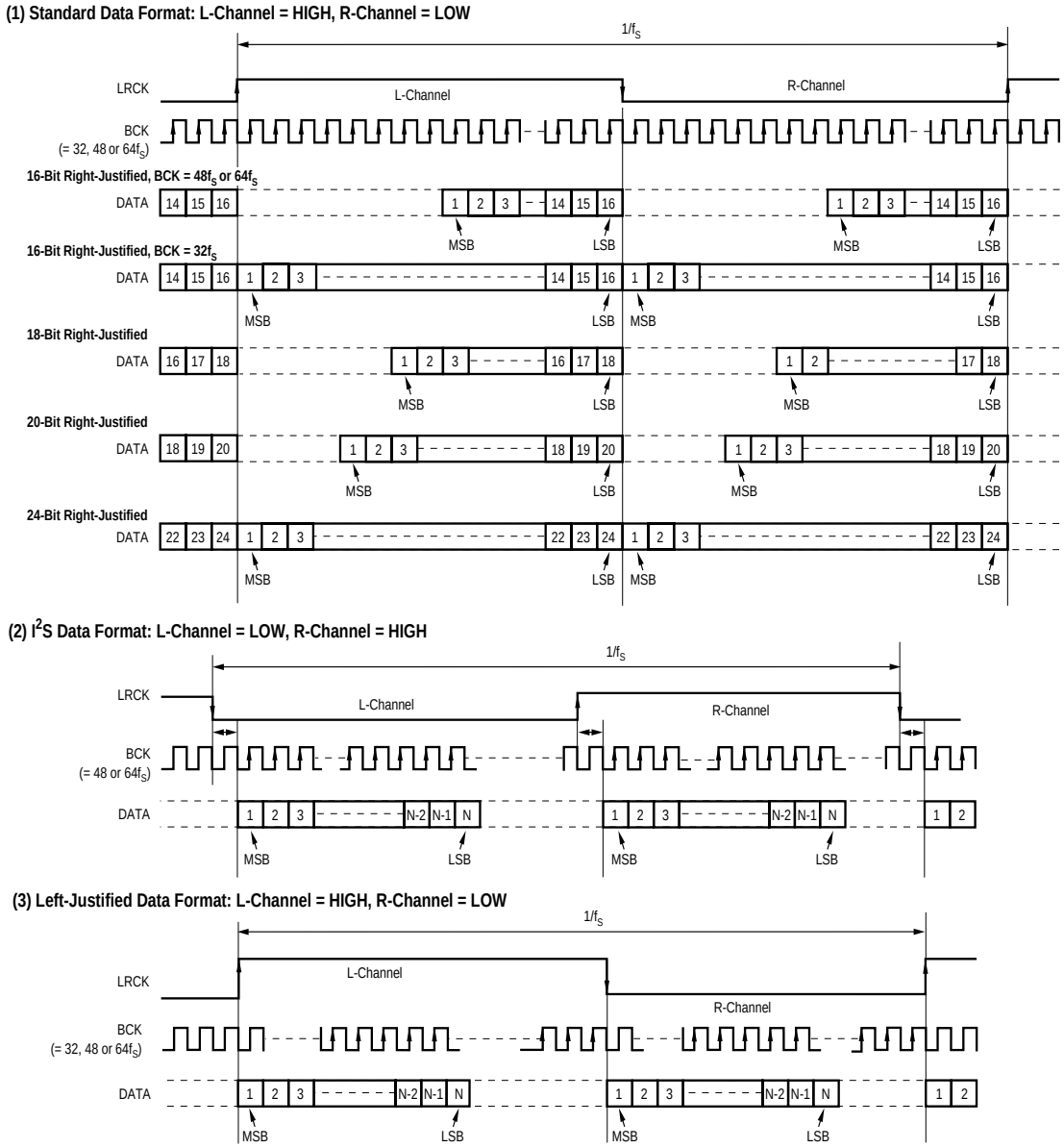
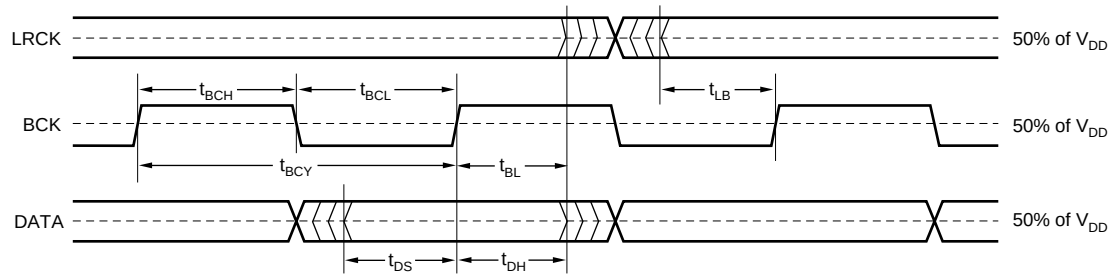


FIGURE 3. Audio Data Input Formats.



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{BCY}	BCK Pulse Cycle Time		32, 48, or 64f_S(1)	
t_{BCH}	BCK High Level Time	35		ns
t_{BCL}	BCK Low Level Time	35		ns
t_{BL}	BCK Rising Edge to LRCK Edge	10		ns
t_{LB}	LRCK Falling Edge to BCK Rising Edge	10		ns
t_{DS}	DATA Set Up Time	10		ns
t_{DH}	DATA Hold Time	10		ns

NOTE: (1) f_S is the sampling frequency (e.g., 44.1kHz, 48kHz, 96kHz, etc.)

FIGURE 4. Audio Interface Timing.

SERIAL CONTROL INTERFACE

The serial control interface is a 3-wire serial port that operates asynchronously to the serial audio interface. The serial control interface is utilized to program the on-chip mode registers. The control interface includes MD (pin 13), MC (pin 14), and ML (pin 15). MD is the serial data input, used to program the mode registers, MC is the serial bit clock, used to shift data into the control port, and ML is the control port latch clock.

REGISTER WRITE OPERATION

All write operations for the serial control port use 16-bit data words. Figure 5 shows the control data word format. The most significant bit must be a “0”. There are seven bits, labeled IDX[6:0], that set the register index (or address) for the write operation. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 6 shows the functional timing diagram for writing the serial control port. ML is held at a logic “1 ” state until a register needs to be written. To start the register write cycle, ML is set to logic “0”. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MD. After the sixteenth clock cycle has completed, ML is set to logic “1” to latch the data into the indexed mode control register.

CONTROL INTERFACE TIMING REQUIREMENTS

See Figure 7 for a detailed timing diagram of the serial control interface. These timing parameters are critical for proper control port operation.

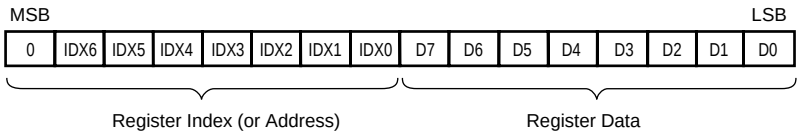


FIGURE 5. Control Data Word Format for MDI.

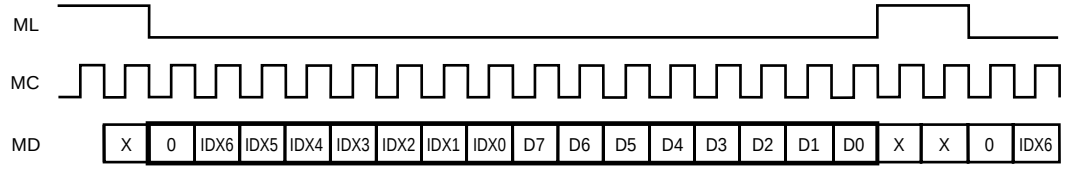


FIGURE 6. Register Write Operation.

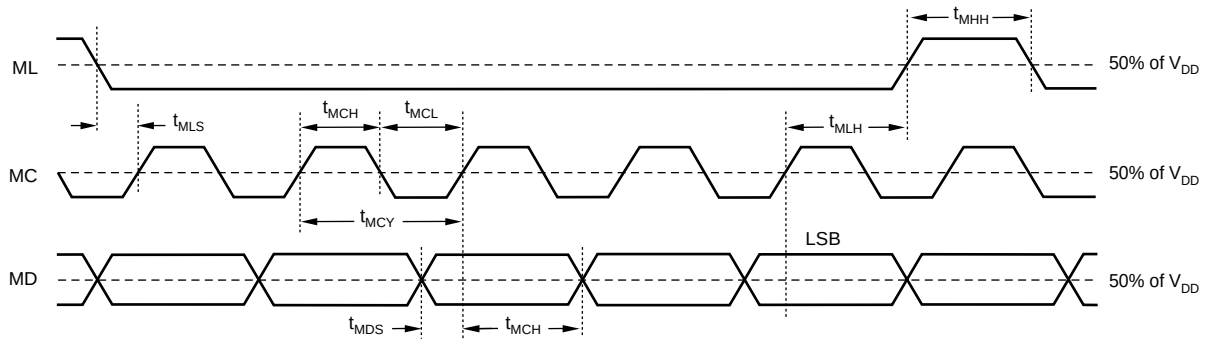
MODE CONTROL REGISTERS

User-Programmable Mode Controls

The PCM1742 includes a number of user-programmable functions that are accessed via control registers. The registers are programmed using the Serial Control Interface that was previously discussed in this data sheet. Table II lists the available mode control functions, along with their reset default conditions and associated register index.

Register Map

The mode control register map is shown in Table III. Each register includes an index (or address) indicated by the IDX[6:0] bits.



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{MCY}	MC Pulse Cycle Time	100			ns
t_{MCL}	MC Low Level Time	50			ns
t_{MCH}	MC High Level Time	50			ns
t_{MHH}	ML High Level Time	Note (2)			ns
t_{MLS}	ML Falling Edge to MC Rising Edge	20			ns
t_{MLH}	ML Hold Time(1)	20			ns
t_{MDH}	MD Hold Time	15			ns
t_{MDS}	MD Set Up Time	20			ns

NOTES: (1) MC rising edge for LSB to ML rising edge. (2) $\frac{3}{256 \bullet f_S}$ sec (min), f_S = Sampling Rate.

FIGURE 7. Control Interface Timing.

FUNCTION	RESET DEFAULT	CONTROL REGISTER	INDEX, IDX[6:0]
Digital Attenuation Control, 0dB to –63dB in 0.5dB Steps	0dB, No Attenuation	16 and 17	AT1[7:0], AT2[7:0]
Soft Mute Control	Mute Disabled	18	MUT[2:0]
Oversampling Rate Control (64 or 128f_S)	64f_S Oversampling	18	OVER
DAC Operation Control	DAC1 and DAC2 Enabled	19	DAC[2:1]
De-Emphasis Function Control	De-Emphasis Disabled	19	DM12
De-Emphasis Sample Rate Selection	44.1kHz	19	DMF[1:0]
Audio Data Format Control	24-Bit Left Justified	20	FMT[2:0]
Digital Filter Roll-Off Control	Sharp Roll-Off	20	FLT
Zero Flag Function Select	L-/R-Channel Independent	22	AZRO
Output Phase Select	Normal Phase	22	DREV
Zero Flag Polarity Select	High	22	ZREV

TABLE II. User-Programmable Mode Controls.

IDX (B8-B14)	REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
10_H	16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
11_H	17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
12_H	18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	OVER	RSV	RSV	RSV	RSV	MUT2	MUT1
13_H	19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	DMF1	DMF0	DM12	RSV	RSV	DAC2	DAC1
14_H	20	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	RSV	RSV	FMT2	FMT1	FMT0
15_H	21	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
16_H	22	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	AZRO	ZREV	DREV

TABLE III. Mode Control Register Map.

REGISTER DEFINITIONS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
Register 17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20

ATx[7:0] **Digital Attenuation Level Setting**

where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

Default Value: $1111\ 1111_B$

Each DAC channel ($V_{OUT}L$ and $V_{OUT}R$) includes a digital attenuator function. The attenuation level may be set from 0dB to –63dB, in 0.5dB steps. Changes in attenuation levels are made by incrementing or decrementing, by one step (0.5dB), for every $8/f_S$ time interval until the programmed attenuator setting is reached. Alternatively, the attenuation level may be set to infinite attenuation, or mute. The attenuation data for each channel can be set individually.

The attenuation level may be set using the formula below.

Attenuation Level (dB) = 0.5 ($ATx[7:0]_{DEC}$ – 255)

where: $ATx[7:0]_{DEC}$ = 0 through 255

for: $ATx[7:0]_{DEC}$ = 0 through 128, the attenuator is set to infinite attenuation.

The following table shows attenuator levels for various settings.

ATx[7:0]	Decimal Value	Attenuator Level Setting
$1111\ 1111_B$	255	0dB, No Attenuation (default)
$1111\ 1110_B$	254	–0.5dB
$1111\ 1101_B$	253	–1.0dB
$1000\ 0011_B$	131	–62.0dB
$1000\ 0010_B$	130	–62.5dB
$1000\ 0001_B$	129	–63.0dB
$1000\ 0000_B$	128	Mute
•	•	•
•	•	•
•	•	•
$0000\ 0000_B$	0	Mute

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	OVER	RSV	RSV	RSV	RSV	MUT2	MUT1

MUTx **Soft Mute Control**

Where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

Default Value: 0

MUTx = 0	Mute Disabled (default)
MUTx = 1	Mute Enabled

The Mute bits, MUT1 and MUT2, are used to enable or disable the Soft Mute function for the corresponding DAC outputs, $V_{OUT}L$ and $V_{OUT}R$. The Soft Mute function is incorporated into the digital attenuators. When Mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When Mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output will be decreased from the current setting to the infinite attenuation setting one attenuator step (0.5dB) at a time. This provides a “pop”-free muting of the DAC output.

OVER **Oversampling Rate Control**

Default Value: 0

OVER = 0	64x Oversampling (default)
OVER = 1	128x Oversampling

The OVER bit is used to control the oversampling rate of the delta-sigma DACs. The OVER = 1 setting is recommended when the oversampling rate is 192kHz (system clock is 128 or $192f_S$).

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	DMF1	DMF0	DM12	RSV	RSV	DAC2	DAC1

DACx **DAC Operation Control**

where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) or $V_{OUT}R$ (x = 2).

Default Value: 0

DACx = 0	DAC Operation Enabled (default)
DACx = 1	DAC Operation Disabled

The DAC operation controls are used to enable and disable the DAC outputs, $V_{OUT}L$ and $V_{OUT}R$. When DACx = 0, the corresponding output will generate the audio waveform dictated by the data present on the DATA pin. When DACx = 1, the corresponding output will be set to the bipolar zero level, or $V_{CC}/2$.

DM12 **Digital De-Emphasis Function Control**

Default Value: 0

DM12 = 0	De-Emphasis Disabled (default)
DM12 = 1	De-Emphasis Enabled

The DM12 bit is used to enable or disable the Digital De-Emphasis function. Refer to the Typical Performance Curves of this data sheet for more information.

DMF[1:0] **Sampling Frequency Selection for the De-Emphasis Function**

Default Value: 00

DMF[1:0]	De-Emphasis Same Rate Selection
00	44.1kHz (default)
01	48kHz
10	32kHz
11	Reserved

The DMF[1:0] bits are used to select the sampling frequency used for the Digital De-Emphasis function when it is enabled.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 20	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	RSV	RSV	FMT2	FMT1	FMT0

FMT[2:0] **Audio Interface Data Format**

Default Value: 101

The FMT[2:0] bits are used to select the data format for the serial audio interface. The following table shows the available format options.

FMT[2:0]	Audio Data Format Selection
000	24-Bit Standard Format, Right-Justified Data
001	20-Bit Standard Format, Right-Justified Data
010	18-Bit Standard Format, Right-Justified Data
011	16-Bit Standard Format, Right-Justified Data
100	I^2S Format, 16- to 24-bits
101	Left-Justified Format, 16- to 24-Bits (default)
110	Reserved
111	Reserved

Register 20 (Cont.)

FLT **Digital Filter Roll-Off Control**

Default Value: 0

FLT = 0	Sharp Roll-Off (default)
FLT = 1	Slow Roll-Off

The FLT bit allows the user to select the digital filter roll-off that is best suited to their application. Two filter roll-off selections are available: Sharp or Slow. The filter responses for these selections are shown in the Typical Performance Curves section of this data sheet.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 22	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	AZRO	ZREV	DREV

DREV **Output Phase Select**

Default Value: 0

DREV = 0	Normal Output (default)
DREV = 1	Inverted Output

The DREV bit is used to set the output phase of $V_{OUT}L$ and $V_{OUT}R$.

ZREV **Zero Flag Polarity Select**

Default Value: 0

ZREV = 0	Zero Flag Pins HIGH at a Zero Detect (default)
ZREV = 1	Zero Flag Pins LOW at a Zero Detect

The ZREV bit allows the user to select the active polarity of Zero Flag pins.

AZRO **Zero Flag Function Select**

Default Value: 0_H

AZRO = 0	L-/R-Channel Independent Zero Flag (default)
AZRO = 1	L-/R-Channel Common Zero Flag

The AZRO bit allows the user to select the function of Zero Flag pins.

AZRO = 0:

Pin11: ZEROR; Zero Flag Output for R-Channel
Pin12: ZEROL; Zero Flag Output for L-Channel

AZRO = 1:

Pin11: ZEROA; Zero Flag Output for L-/R-Channel
Pin12: NA; No Assign

ANALOG OUTPUTS

The PCM1742 includes two independent output channels: $V_{OUT}L$ and $V_{OUT}R$. These are unbalanced outputs, each capable of driving 3.1Vp-p typical into a 5kΩ AC-coupled load. The internal output amplifiers for $V_{OUT}L$ and $V_{OUT}R$ are biased to the DC common-mode (or bipolar zero) voltage, equal to $V_{CC}/2$.

The output amplifiers include an RC continuous-time filter that helps to reduce the out-of-band noise energy present at the DAC outputs, due to the noise shaping characteristics of the PCM1742's delta-sigma DACs. The frequency response of this filter is shown in Figure 8. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for many applications, therefore, an external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the Applications Information section of this data sheet.

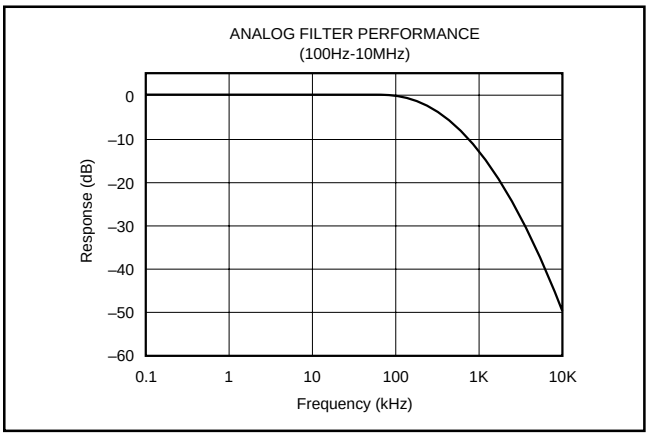


FIGURE 8. Output Filter Frequency Response.

V_{COM} OUTPUT

One unbuffered common-mode voltage output pin, V_{COM} (pin 10), is brought out for decoupling purposes. This pin is nominally biased to a DC voltage level equal to $V_{CC}/2$. This pin may be used to bias external circuits. An example of using the V_{COM} pin for external biasing applications is shown in Figure 9.

ZERO FLAGS

Zero Detect Condition

Zero Detection for each output channel is independent from the other. If the data for a given channel remains at a "0" level for 1024 sample periods (or LRCK clock periods), a Zero Detect condition exists for that channel.

Zero Output Flags

Given that a Zero Detect condition exists for one or more channels, the Zero Flag pins for those channels will be set to a logic "1" state. There are Zero Flag pins for each channel: ZEROL (pin 12) and ZEROR (pin 11). These pins can be used

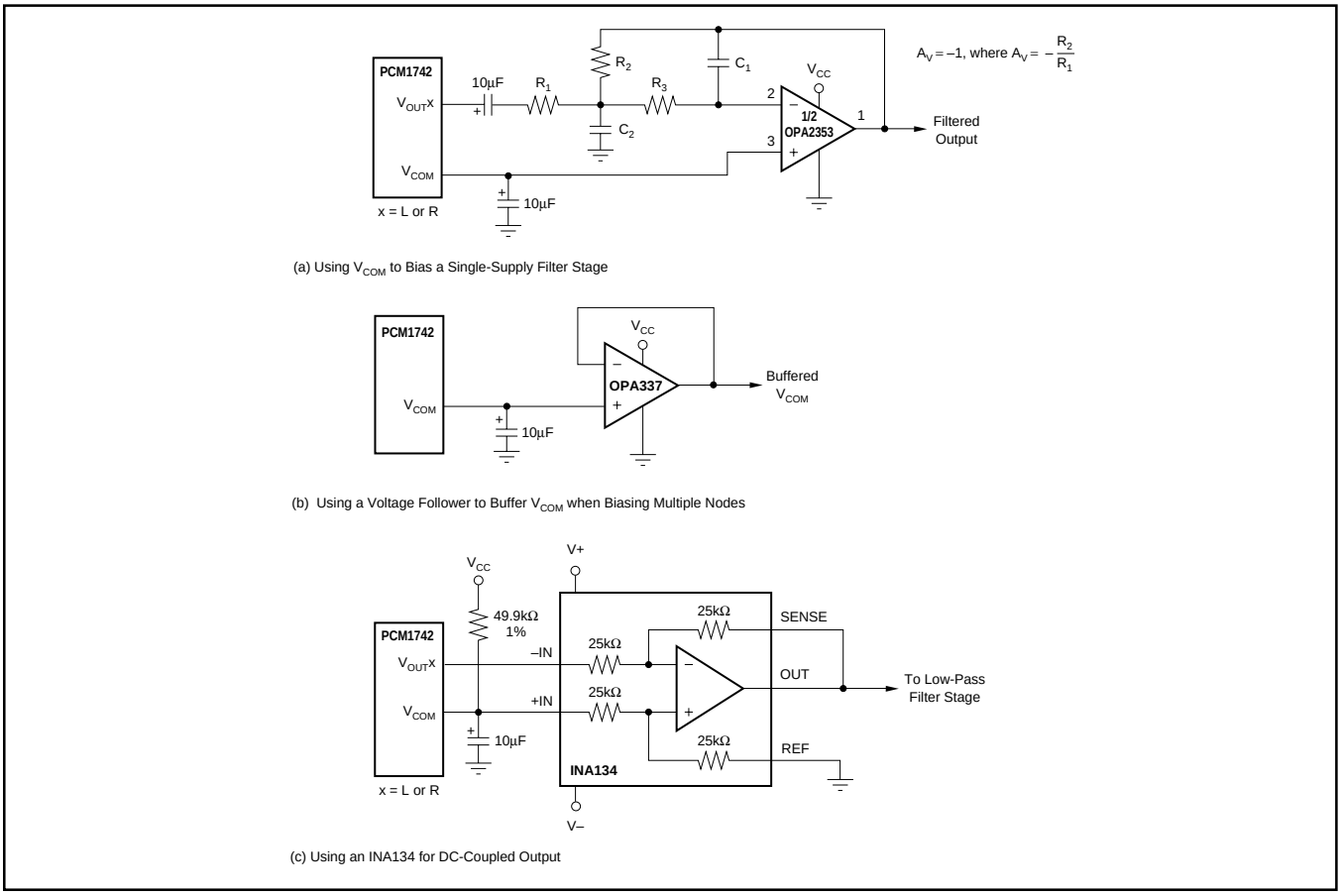


FIGURE 9. Biasing External Circuits Using the V_{COM} Pin.

to operate external mute circuits, or used as status indicators for a microcontroller, audio signal processor, or other digitally controlled functions.

The active polarity of Zero Flag output can be inverted by setting the ZREV bit of Control Register 22 to "1". The reset default is active high output, or ZREV = 0.

The L-channel and R-channel common Zero Flag can be selected by setting the AZRO bit of Control Register 22 to "1". The reset default is L-channel and R-channel independent Zero Flag, or AZRO = 0.

APPLICATIONS INFORMATION

CONNECTION DIAGRAMS

A basic connection diagram is shown in Figure 11, with the necessary power-supply bypassing and decoupling components. Texas Instruments recommends using the component values shown in Figure 11 for all designs.

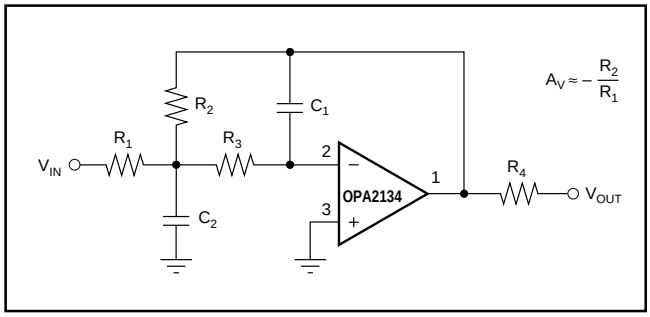


FIGURE 10. Dual-Supply Filter Circuit.

The use of series resistors (22Ω to 100Ω) are recommended for the SCK, LRCK, BCK, and DATA inputs. The series resistor combines with stray PCB and device input capacitance to form a low-pass filter that reduces high-frequency noise emissions and helps to dampen glitches and ringing present on clock and data lines.

POWER SUPPLIES AND GROUNDING

The PCM1742 requires a +5V analog supply (V_{CC}) and a +3.3V digital supply (V_{DD}). The +5V supply (V_{CC}) is used to power the DAC analog and output filter circuitry, while the +3.3V (V_{DD}) supply is used to power the digital filter and serial interface circuitry. For best performance, the +3.3V (V_{DD}) supply should be derived from the +5V (V_{CC}) supply using a linear regulator, as shown in Figure 11. The REG1117-3.3 from Texas Instruments is an ideal choice for this application.

Proper power-supply bypassing is shown in Figure 11. The 10µF capacitors should be tantalum or aluminum electrolytic.

DAC OUTPUT FILTER CIRCUITS

Delta-sigma DACs utilize noise-shaping techniques to improve in-band Signal-to-Noise Ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist Frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide the optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

Figures 9(a) and 10 show the recommended external low-pass active filter circuits for single- and dual-supply applications. These circuits are second-order Butterworth filters using a Multiple FeedBack (MFB) circuit arrangement that reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, please refer to Burr-Brown Applications Bulletin #34 AB-034 (SBFA001), available from our web site at http://www.ti.com.

Since the overall system performance is defined by the quality of the DACs and their associated analog output circuitry, high-quality audio op amps are recommended for the active filters. The OPA2353 and OPA2134 dual op amps from Texas Instruments are recommended for use with the PCM1742, see Figures 9(a) and 10.

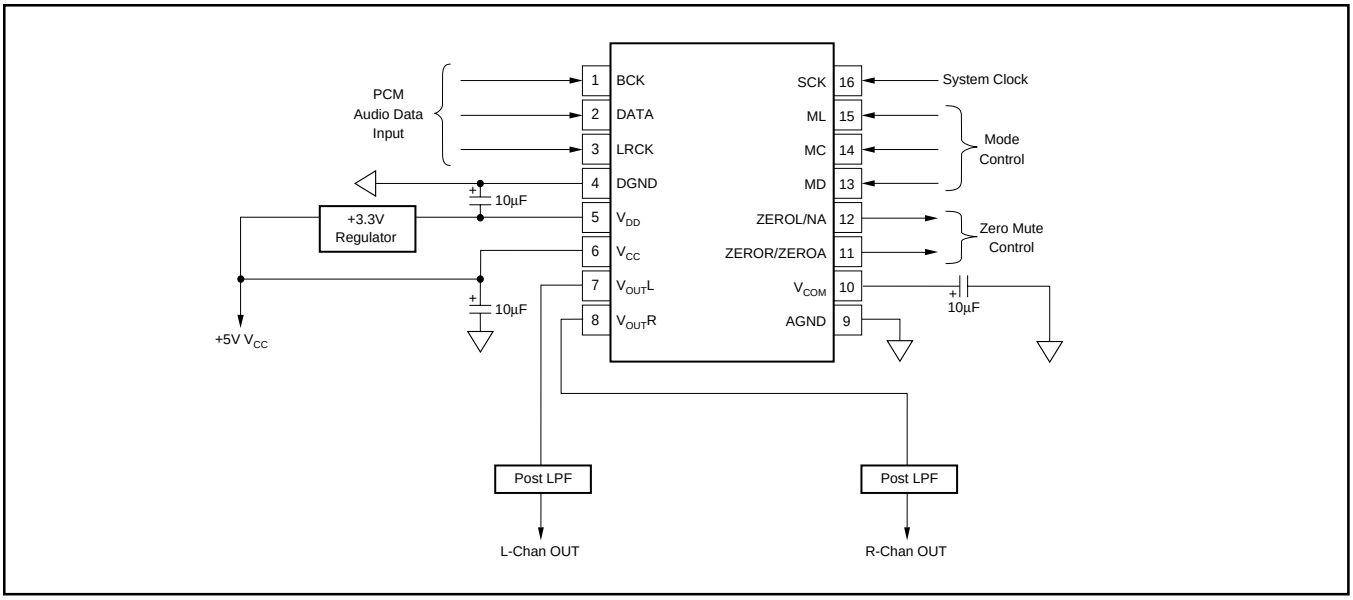


FIGURE 11. Basic Connection Diagram.

PCB LAYOUT GUIDELINES

A typical PCB floor plan for the PCM1742 is shown in Figure 12. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1742 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM1742. In cases where a common +5V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital +5V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 13 shows the recommended approach for single-supply applications.

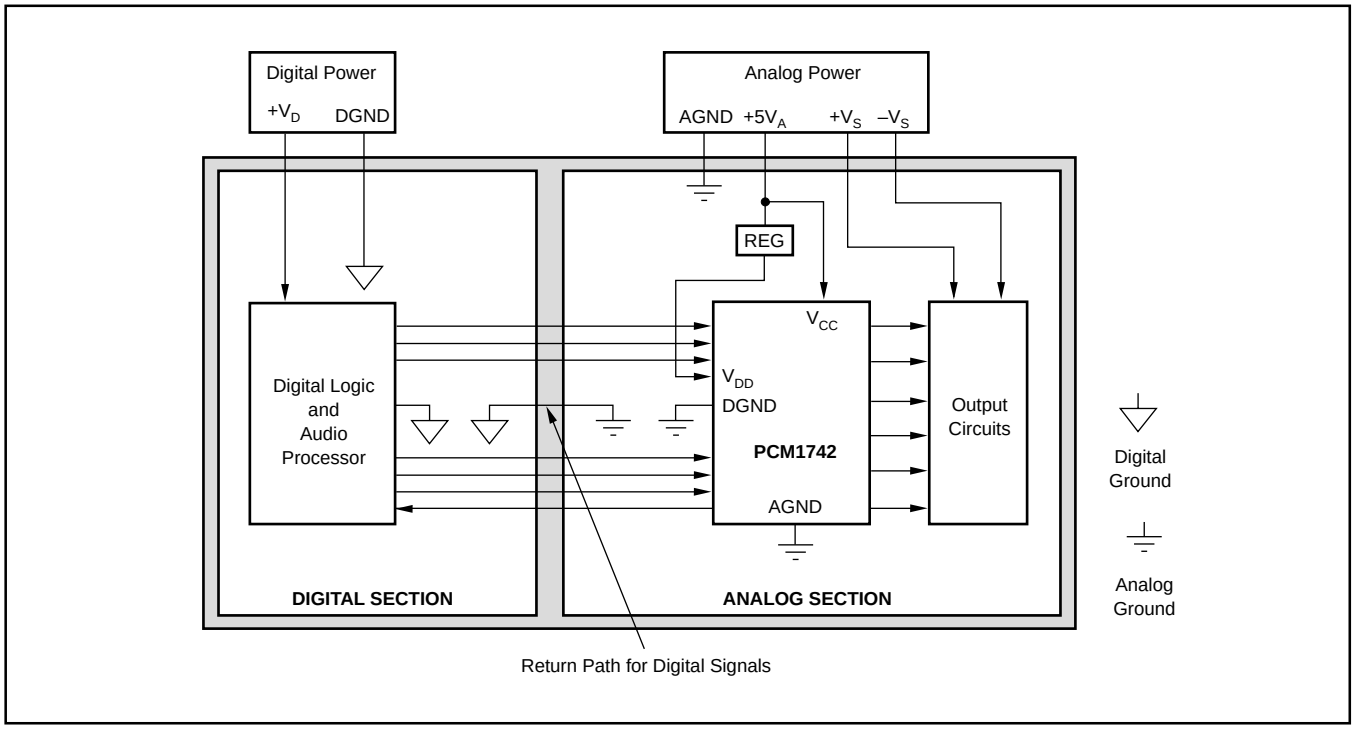


FIGURE 12. Recommended PCB Layout.

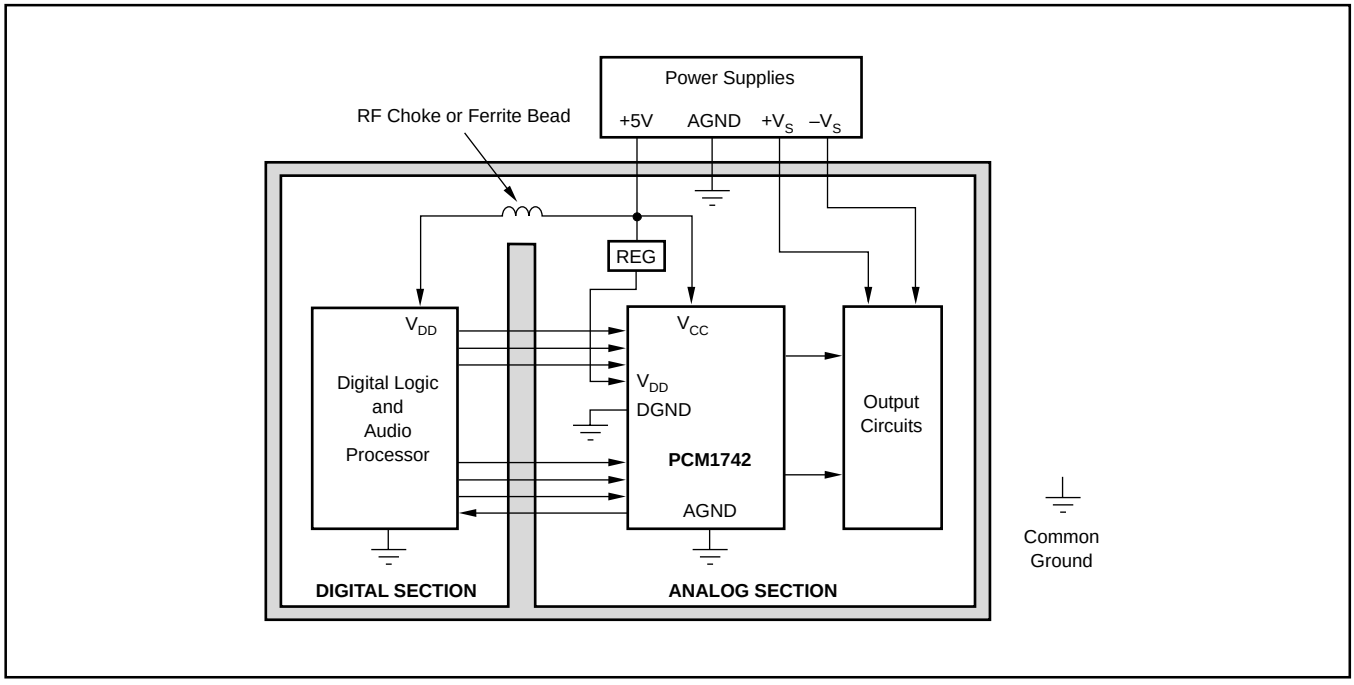


FIGURE 13. Single-Supply PCB Layout.

THEORY OF OPERATION

The delta-sigma section of the PCM1742 is based on an 8-level amplitude quantizer and a fourth-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format. A block diagram of the 8-level delta-sigma modulator is shown in Figure 14. This 8-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2-level) delta-sigma modulator. The combined oversampling rate of the delta-sigma modulator and the interpolation filter is $64f_S$.

The theoretical quantization noise performance of the 8-level delta-sigma modulator is shown in Figure 15. The enhanced multilevel delta-sigma architecture also has advantages for input clock jitter sensitivity due to the multilevel quantizer, with the simulated jitter sensitivity, as shown in Figure 16.

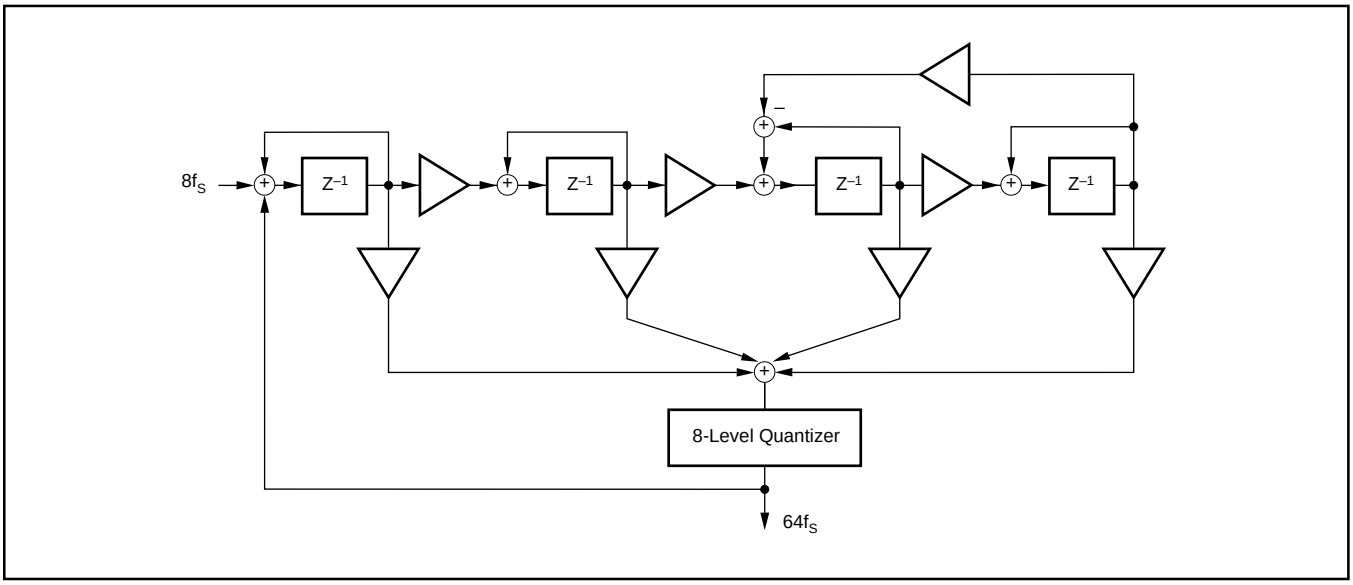


FIGURE 14. 8-Level Delta-Sigma Modulator.

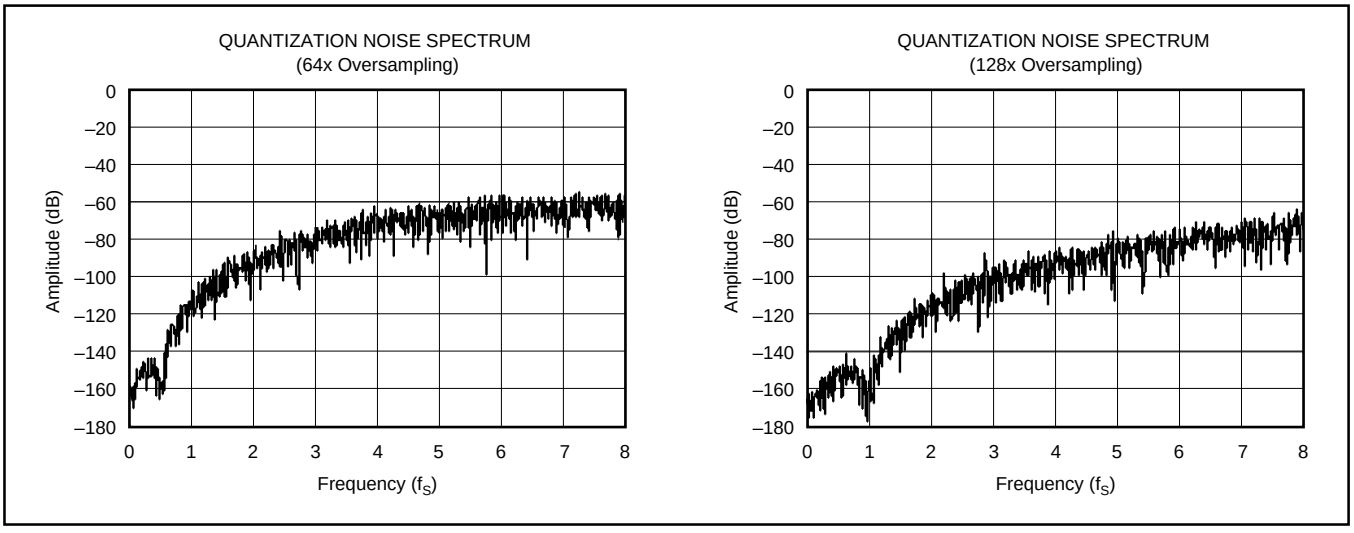


FIGURE 15. Quantization Noise Spectrum.

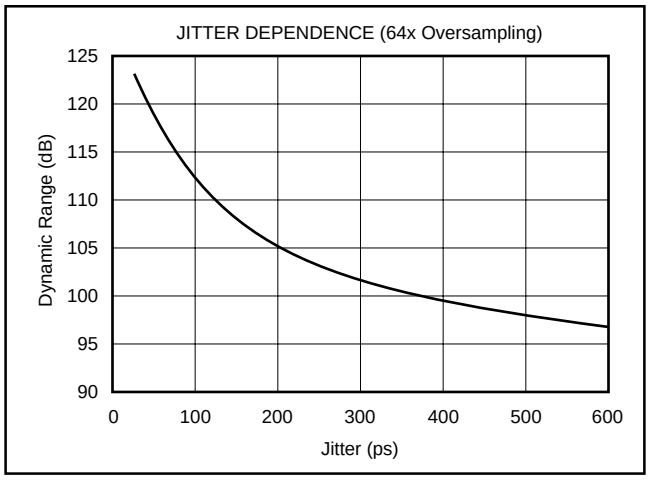


FIGURE 16. Jitter Sensitivity.

KEY PERFORMANCE PARAMETERS AND MEASUREMENT

This section provides information on how to measure key dynamic performance parameters for the PCM1742. In all cases, an Audio Precision System Two Cascade or equivalent audio measurement system is utilized to perform the testing.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion + Noise (THD+N) is a significant figure of merit for audio DACs, since it takes into account both harmonic distortion and all noise sources within a specified measurement bandwidth. The true rms value of the distortion and noise is referred to as THD+N. Figure 17 shows the test setup for THD+N measurements.

For the PCM1742, THD+N is measured with a full-scale, 1kHz digital sine wave as the test stimulus at the input of the DAC. The digital generator is set to a 24-bit audio word length and a sampling frequency of 44.1kHz or 96kHz. The digital generator output is taken from the unbalanced S/PDIF connector of the measurement system. The S/PDIF data is transmitted via a coaxial cable to the digital audio receiver on the DEM-DAI1742 demo board. The receiver is then configured to output 24-bit data in either I^2S or left-justified data format. The DAC audio interface format is programmed to match the receiver output format. The analog output is then taken from the DAC post filter and connected to the analog analyzer input of the measurement system. The analog input is band limited using filters resident in the analyzer. The resulting THD+N is measured by the analyzer and displayed by the measurement system.

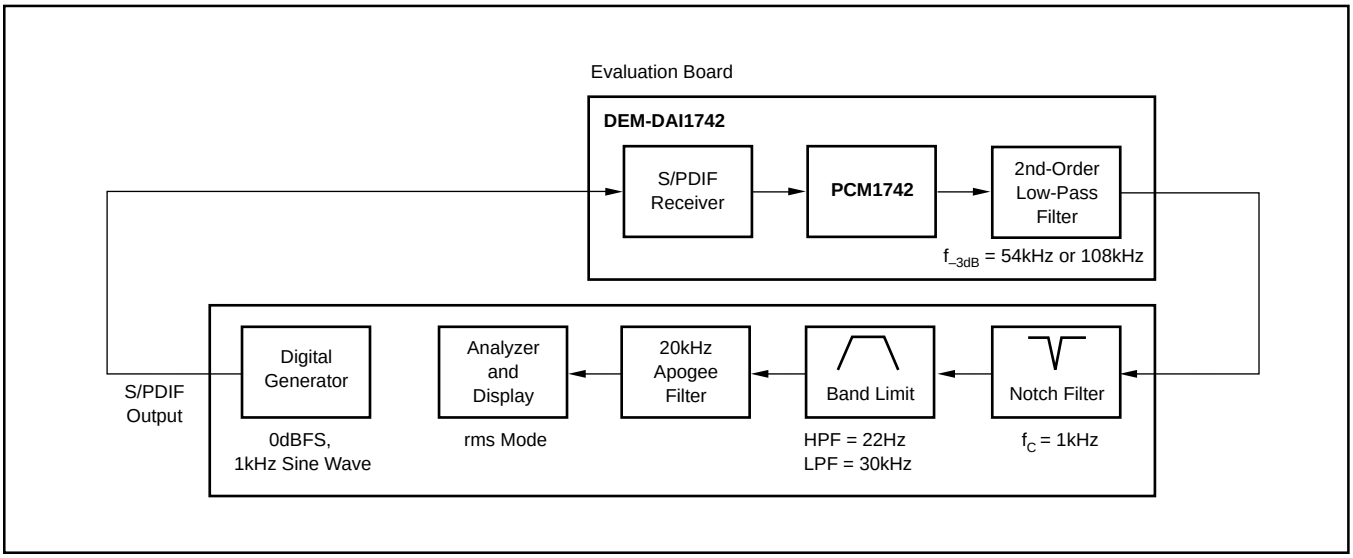


FIGURE 17. Test Setup for THD+N Measurements.

DYNAMIC RANGE

Dynamic range is specified as A-Weighted, THD+N measured with a –60dBFS, 1kHz digital sine wave stimulus at the input of the DAC. This measurement is designed to give a good indicator of how the DAC will perform given a low-level input signal.

The measurement setup for the dynamic range measurement is shown in Figure 18, and is similar to the THD+N test setup discussed previously. The differences include the band limit filter selection, the additional A-Weighting filter, and the –60dBFS input level.

IDLE CHANNEL SIGNAL-TO-NOISE RATIO

The SNR test provides a measure of the noise floor of the DAC. The input to the DAC is all "0"s data, and the DAC's Infinite Zero Detect Mute function must be disabled (default condition at power up for the PCM1742). This ensures that the delta-sigma modulator output is connected to the output amplifier circuit so that idle tones (if present) can be observed and effect the SNR measurement. The dither function of the digital generator must also be disabled to ensure an all "0"s data stream at the input of the DAC. The measurement setup for SNR is identical to that used for dynamic range, with the exception of the input signal level (see the notes provided in Figure 18).

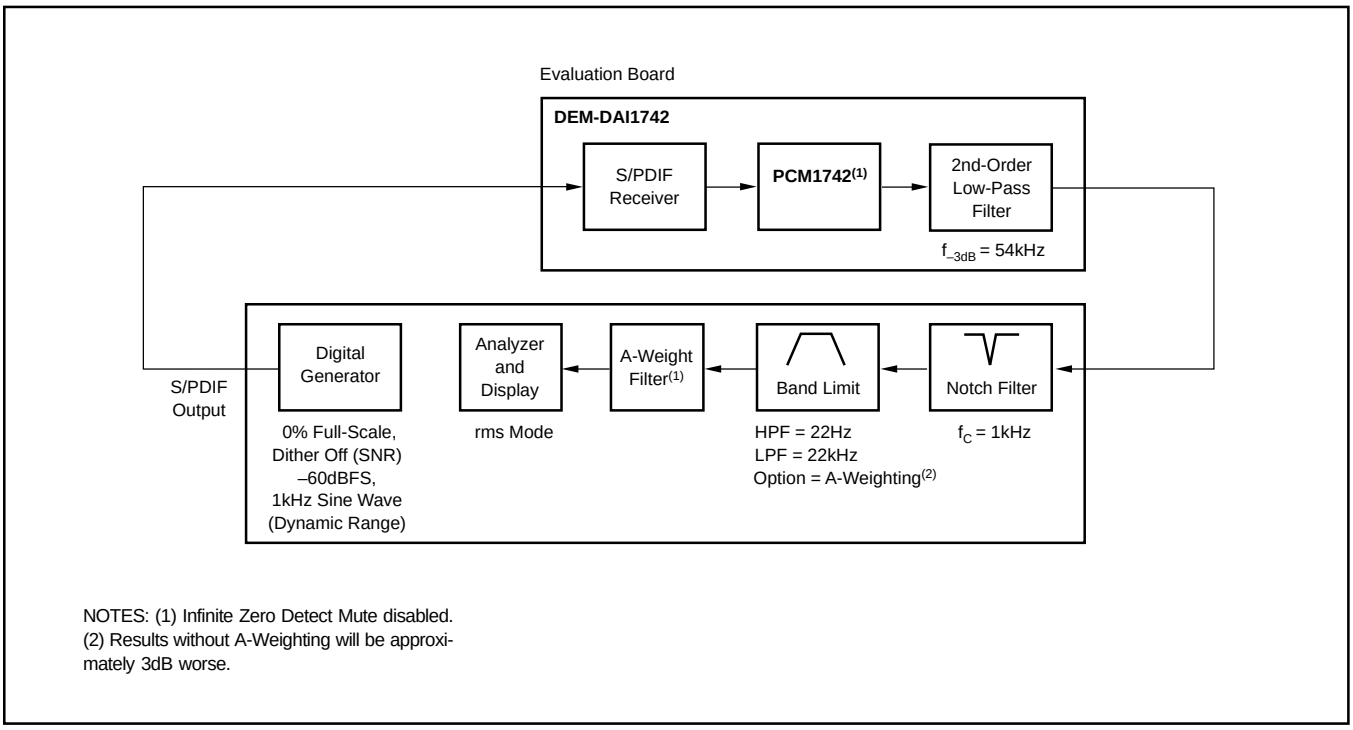


FIGURE 18. Test Setup for Dynamic Range and SNR Measurements.

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
PCM1742E	ACTIVE	SSOP	DBQ	16	98
PCM1742E/2K	ACTIVE	SSOP	DBQ	16	2000
PCM1742KE	ACTIVE	SSOP	DBQ	16	98
PCM1742KE/2K	ACTIVE	SSOP	DBQ	16	2000

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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