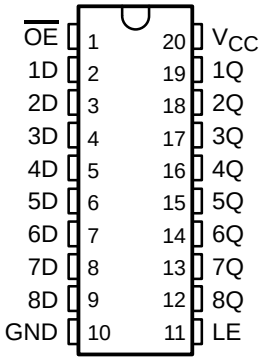
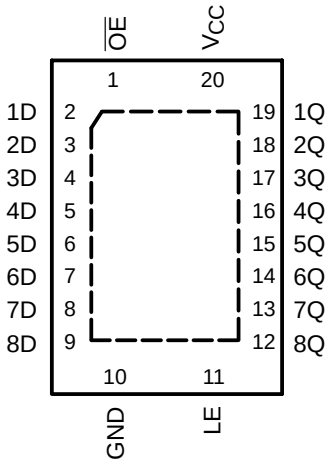
- **Operate From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 6.9 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

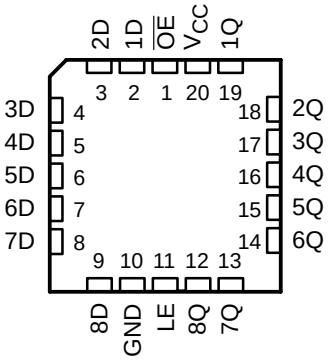
SN54LVC573A . . . J OR W PACKAGE
SN74LVC573A . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN74LVC573A . . . RGY PACKAGE
(TOP VIEW)



SN54LVC573A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74LVC573AN	SN74LVC573AN
	QFN – RGY	Tape and reel	SN74LVC573ARGYR	LC573A
	SOIC – DW	Tube	SN74LVC573ADW	LVC573A
		Tape and reel	SN74LVC573ADWR	
	SOP – NS	Tape and reel	SN74LVC573ANSR	LVC573A
	SSOP – DB	Tape and reel	SN74LVC573ADBR	LC573A
	TSSOP – PW	Tape and reel	SN74LVC573APWR	LC573A
	TVSOP – DGV	Tape and reel	SN74LVC573ADGVR	LC573A
	VFBGA – GQN	Tape and reel	SN74LVC573AGQNR	LC573A
–55°C to 125°C	CDIP – J	Tube	SNJ54LVC573AJ	SNJ54LVC573AJ
	CFP – W	Tube	SNJ54LVC573AW	SNJ54LVC573AW
	LCCC – FK	Tube	SNJ54LVC573AFK	SNJ54LVC573AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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description/ordering information (continued)

The SN54LVC573A octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC573A octal transparent D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

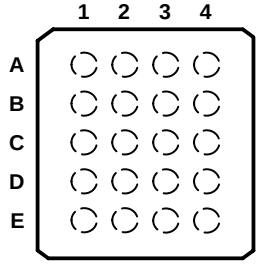
$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

GQN PACKAGE
(TOP VIEW)



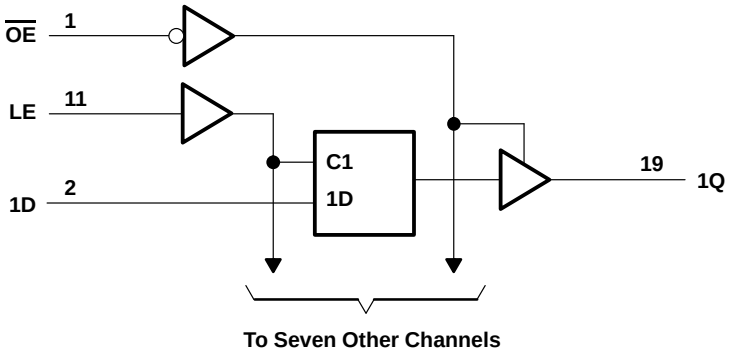
terminal assignments

	1	2	3	4
A	1D	$\overline{OE}$	V_{CC}	1Q
B	3D	3Q	2D	2Q
C	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
E	GND	8D	LE	8Q

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, N, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 6.5 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O
(see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Continuous output current, I_O . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . . 70°C/W
(see Note 3): DGV package . . . . . 92°C/W
(see Note 3): DW package . . . . . 58°C/W
(see Note 3): GQN package . . . . . 76°C/W
(see Note 3): N package . . . . . 69°C/W
(see Note 3): NS package . . . . . 60°C/W
(see Note 3): PW package . . . . . 83°C/W
(see Note 4): RGY package . . . . . 37°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LVC573A		SN74LVC573A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V			$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V			1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V				$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V				0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V				–4	mA
		V_{CC} = 2.3 V				–8	
		V_{CC} = 2.7 V		–12		–12	
		V_{CC} = 3 V		–24		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V				4	mA
		V_{CC} = 2.3 V				8	
		V_{CC} = 2.7 V		12		12	
		V_{CC} = 3 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			6		6	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	SN54LVC573A			SN74LVC573A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	I_{OH} = –100 μA		1.65 V to 3.6 V				V_{CC}–0.2			V
			2.7 V to 3.6 V	V_{CC}–0.2						
	I_{OH} = –4 mA		1.65 V				1.2			
	I_{OH} = –8 mA		2.3 V				1.7			
	I_{OH} = –12 mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	I_{OH} = –24 mA		3 V	2.2			2.2			
V_{OL}	I_{OL} = 100 μA		1.65 V to 3.6 V						0.2	V
			2.7 V to 3.6 V			0.2				
	I_{OL} = 4 mA		1.65 V						0.45	
	I_{OL} = 8 mA		2.3 V						0.7	
	I_{OL} = 12 mA		2.7 V			0.4			0.4	
	I_{OL} = 24 mA		3 V			0.55			0.55	
I_I	V_I = 0 to 5.5 V		3.6 V			±5			±5	μA
I_{off}	V_I or V_O = 5.5 V		0			±10			±10	μA
I_{OZ}	V_O = 0 to 5.5 V		3.6 V			±15			±10	μA
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			10			10	μA
	3.6 V ≤ V_I ≤ 5.5 V‡					10			10	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500			500	μA
C_i	V_I = V_{CC} or GND		3.3 V		4			4		pF
C_o	V_O = V_{CC} or GND		3.3 V		5.5			5.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVC573A				UNIT
		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	3.3		3.3		ns
t_{su}	Setup time, data before LE↓	2		2		ns
t_h	Hold time, data after LE↓	2.5		2.5		ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN74LVC573A								UNIT
		V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	†		†		3.3		3.3		ns
t_{su}	Setup time, data before LE↓	†		†		2		2		ns
t_h	Hold time, data after LE↓	†		†		1.5		1.5		ns

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC573A				UNIT
			V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t_{pd}	D	Q		7.7	1	6.9	ns
	LE			8.4	1	7.7	
t_{en}	$\overline{OE}$	Q		8.5	1	7.5	ns
t_{dis}	$\overline{OE}$	Q		7	0.5	6.7	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC573A								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	†	†	†	†		7.7	1.5	6.9	ns
	LE		†	†	†	†		8.4	2	7.7	
t_{en}	$\overline{OE}$	Q	†	†	†	†		8.5	1.5	7.5	ns
t_{dis}	$\overline{OE}$	Q	†	†	†	†		7	1.6	6.5	ns
$t_{sk(o)}$										1	ns

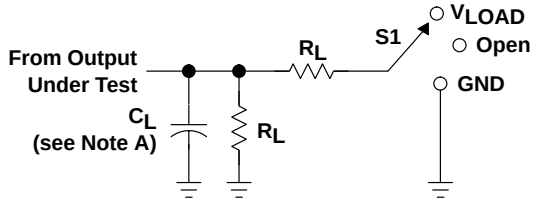
† This information was not available at the time of publication.

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	f = 10 MHz	†	†	37	pF
		Outputs disabled		†	†	4	

† This information was not available at the time of publication.

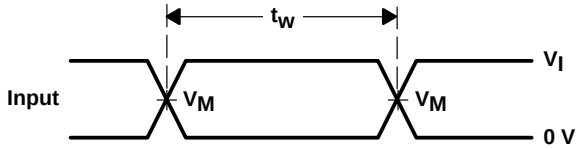
PARAMETER MEASUREMENT INFORMATION



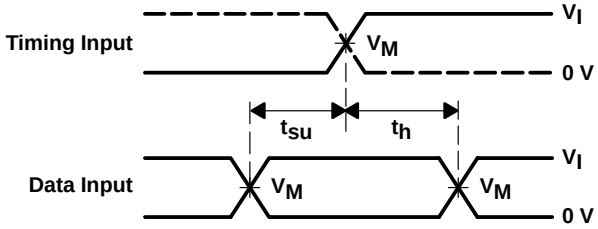
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

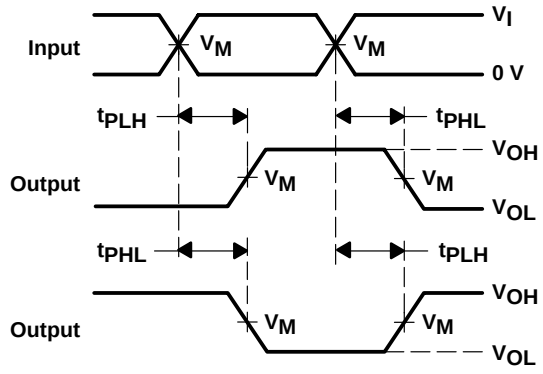
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



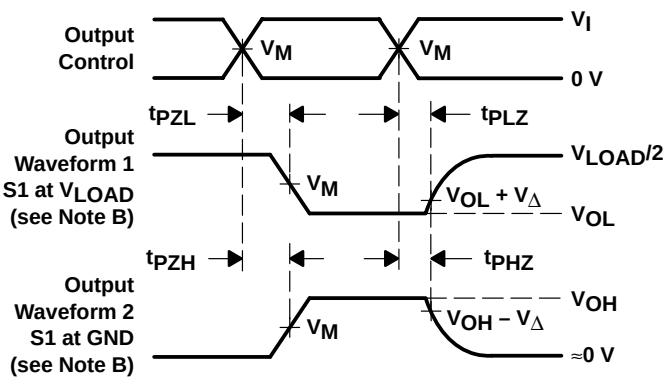
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265