Application Note:AN_SY6982C

High Efficiency, 2A, Two-Cell Boost Li-Ion Battery Charger

Preliminary Specification

General Description

SY6982C is a 3.0-5.5V_{IN}, 2A two-cell synchronous boost Li-Ion battery charger integrates 1MHz switching frequency and full protection functions. The charge current up to 2A can be programmed by using the external resistor for different portable applications and indicates the charger current information simultaneous. It also has a programmable charge timeout and adaptive input current limit with selectable threshold for safety battery charge operation. SY6982C can disconnect output when there is output short circuit or shutdown happens. It consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

SY6982C along with small QFN3x3 footprint provides small PCB area application.

Ordering Information

SY6982 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6982CQDC	QFN3x3-16	

Features

- Low Profile QFN3x3 Package for Portable Applications
- Integrated Synchronous Boost with 18V Rating Low R_{DSON} FETs for High Charge Efficiency
- Trickle Current / Constant Current / Constant Voltage Charge Mode
- Adaptive Input Current Limit with selectable threshold
- Maximum 2A Constant Charge Current
- Charge Current Information Indication.
- Programmable Charge Timeout
- Programmable Constant Charge Current
- Constant Voltage Selectable
- Thermal Regulation Protection
- External Shutdown Function
- Input Voltage UVLO and OVP
- Over Temperature Protection
- Output Short Circuit Protection
- Charge Status Indication
- Normal Synchronous Boost Operation When Battery Removed

Applications

- Cellular Telephones, PDA, MP3 Players, MP4 Players
- Digital Cameras
- Bluetooth Applications
- PSP Game Players, NDS Game Players
- Notebook

Typical Applications

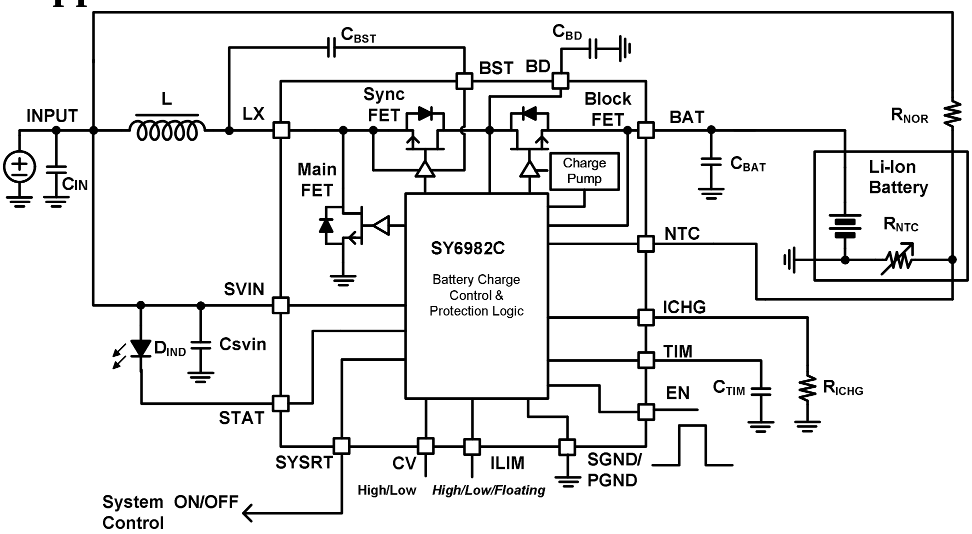
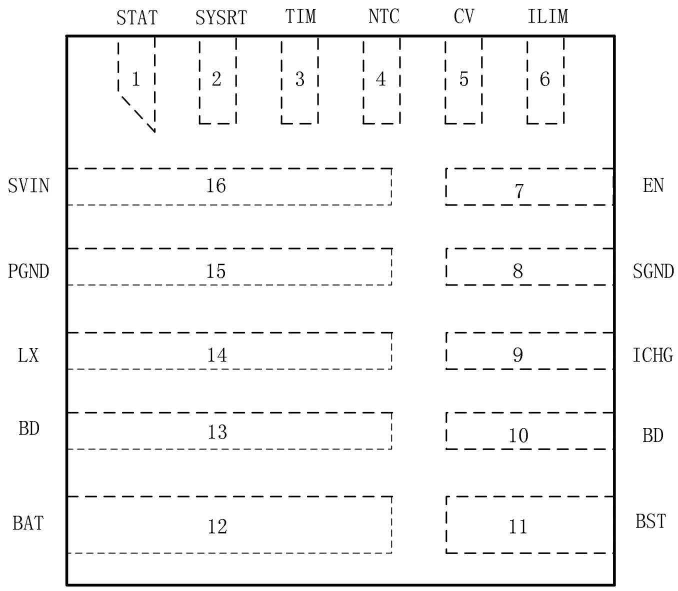


Figure1. Schematic Diagram

Pinout (top view)



(QFN3x3-16)

Top Mark: **XX***xyz*, **(**Device code: XX, ***x=year code, y=week code, z= lot number code*****)**

Name	Pin Number	Description
LX	14	Switch node pin. Connect to external inductor.
STAT	1	Charge status indication pin. It is open drain output pin and pull high to S_{VIN} thru a LED to indicate the charge in process. When the charge is done, LED is off.
SVIN	16	Analog power input pin. Connect a MLCC from this pin to ground to decouple high harmonic noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage area.
CV	5	Battery CV voltage selection pin. Pull down for 8.4V cell voltage and pull up for 8.7V cell voltage.
ILIM	6	Adaptive input current limit setting Pin. Select the permitted maximum input voltage drop to trigger the input current limit function. Pull high for 500mV voltage drop, pull low for 375mV, floating for 250mV.
TIM	3	Charge time limit pin. Connect this pin with a capacitor to ground. Internal current source charge the capacitor for charge time limit. TC charge time limit is about 1/10 of CC charge time.
ICHG	9	Charge current program pin, pull down to GND with a resistor $R_{ICHG.}$ The mirror current about 1/10000 of the blocking FET current will dump into the external resitor thru ICHG pin and compared to the internal reverence 1V. So I_{CC}=(1V/ R_{ICHG})x10000, I_{TC}=(1V/ R_{ICHG})x1000.
NTC	4	Thermal protection pin. UTP threshold is typical 75%V_{SVIN} and OTP threshold is typical 25% V_{SVIN}. Pull up to SVIN can disable charge logic and make the IC operate as normal boost regulator. Pull down to ground can shut down the IC.
BAT	12	Battery positive pin.
BST	11	Boost-Strap pin. Supply Rectified FET’s gate driver. Decouple this pin to LX with 0.1uF ceramic cap.
BD	10, 13	Connect to the Drain of internal Blocking FET. Bypass at least 4.7uF ceramic cap to GND.
EN	7	Enable control pin. High logic for enable on, and low logic for enable off.

SYSRT	2	System ON/OFF control pin. When V_{BAT} is lower than 6V, SYSRT pin outputs low logic to turn off the system operation; when V_{BAT} is high than 6V, SYSRT pin outputs high logic to turn on the system operation.
SGND	8	Signal ground pin.
PGND	15	Power ground pin.

Absolute Maximum Ratings

SVIN, BAT, LX, NTC, STAT, BD, EN, ICHG, CV, ILIM-- 18V
TIM -- 4V
BST-LX Voltage --- 4V
LX Pin current continuous -- 5A
Power Dissipation, P_D @ T_A = 25°C, QFN3X3-- TBD
Package Thermal Resistance
θ_{JA} --- TBD
θ_{JC} --- TBD
Junction Temperature Range -- -40°C to +125°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions

SVIN --- 3V to 5.5V
BAT, LX, NTC, STAT, BD, EN, ICHG, CV, ILIM --- -0.3V to 16V
TIM --- -0.3V to 3.3V
LX Pin current continuous -- 5A
Junction Temperature Range -- -40°C to 125°C
Ambient Temperature Range --- -40°C to 85°C

Electrical Characteristics

(T_A=25°C, V_{IN}=5V, GND=0V, C_{IN}=4.7uF, L=0.68uH, R_{ICHG}=10kΩ, C_{TIM}=470nF, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bias Supply (V_{SVIN})						
V_{SVIN}	Supply voltage		3		16	V
V_{UVLO}	V_{SVIN} under voltage lockout threshold	V_{SVIN} rising and measured from V_{SVIN} to GND			2.9	V
ΔV_{UVLO}	V_{SVIN} under voltage lockout hysteresis	Measured from V_{SVIN} to GND		100		mV
V_{OVP}	Input overvoltage protection	V_{SVIN} rising and measured from V_{SVIN} to GND	6			V
ΔV_{OVP}	Input overvoltage protection hysteresis	Measured from V_{SVIN} to GND		0.5		V
Quiescent Current						
I_{BAT}	Battery discharge current	Shutdown IC			25	uA
I_{IN}	Input quiescent current	Disable Charge			1.5	mA
Oscillator and PWM(TBD)						
f_{SW}	Switching frequency			1000		kHz
T_{MINOFF}	Main N-FET minimum off time	With 16V rating		100		ns
T_{MAXOFF}	Main N-FET maximum off time	With 16V rating		30		us
T_{MINON}	Main N-FET minimum on time	With 16V rating		100		ns
Power MOSFET						
R_{NFET_M}	$R_{DS(ON)}$ of Main N-FET			80		mΩ
R_{NFET_R}	$R_{DS(ON)}$ of Rectified N-FET			40		mΩ
R_{NFET_B}	$R_{DS(ON)}$ of Blocking N-FET			40		mΩ
Voltage Regulation						
V_{CV}	2-Cell CV charge mode voltage	V_{CV}<1V	8.32	8.40	8.48	V
		V_{CV}>2V	8.62	8.70	8.78	
$V_{CV1/2H}$	High level logic for CV1/2		2			V
$V_{CV1/2L}$	Low level logic for CV1/2				1	V
ΔV_{RCH}	2-Cell Recharge Voltage		100	200	300	mV
V_{TRK}	2-cell TC charge mode battery voltage threshold	V_{BAT} rising edge threshold	5.5	5.6	5.7	V
Battery Connect Detection						
V_{DET}	NTC voltage threshold for Battery detect	NTC Falling Edge	85%		95%	V_{SVIN}
t_{DET}	Detect delay time		30	35	40	ms
Charge Current						
	Internal charge current accuracy for Constant Current Mode	I_{CC}=1000mA	-10%		10%	
	Internal charge current accuracy for Trickle Current Mode	I_{TC}=100mA	-50%		50%	
I_{TERM}	Termination current	I_{CC}=1000mA	50	100	150	mA
Output Voltage OVP						
V_{OVP}	Output voltage OVP threshold		105%	110%	115%	V_{CV}
Input Current Limit						
$V_{DISSDRP}$	Vin drop for slow CC REF discharge Voltage Threshold	Float ILIM		250		mV
		Pull low ILIM		375		
		Pull high ILIM		500		

Δ V_{DISS}	Slow Discharge Voltage Hysteresis	Positive edge		50		mV
V_{DISF}	Vin drop for fast CC REF discharge Voltage Threshold	Float ILIM		500		mV
		Pull low ILIM		750		
		Pull high ILIM		1000		
Δ V_{DISF}	Fast Discharge Voltage Hysteresis			50		mV
Timer						
T_{TC}	Trickle current charge timeout	C_{TIM}=330nF	0.425	0.5	0.575	hour
T_{CC}	Constant current charge timeout		3.825	4.5	5.175	hour
T_{MC}	Charge mode change delay time			30		ms
T_{TERM}	Termination delay time			30		ms
T_{RCHG}	Recharge time delay			30		ms
Short Circuit Protection						
V_{SHORT}	Output short protection threshold		1.70	2.00	2.30	V
System ON/OFF Control						
V_{HSYSRT}	High logic of system ON/OFF control		2.1			V
V_{LSYSRT}	Low logic of system ON/OFF control				0.6	V
V_{HYSSYS}	Hysteresis for positive and negative edge			100		mV
Linear charger Mode						
I_{LCHG}	Battery Charger current when the blocking FET is in linear mode	V_{BAT}<V_{SHORT}		5%		I_{CC}
I_{LPEAK}	Peak linear current when Battery is absent			1		A
V_{BD}	Bus voltage regulation		5.8	6	6.2	V
V_{TRON}	Blocking FET fully turn on threshold $V_{TRON}=V_{BAT}-V_{IN}$	V_{BAT} > V_{TRK}		100		mV
Enable ON/OFF Control						
V_{ENH}	High level logic for enable control		1.5			V
V_{ENL}	Low level logic for enable control				0.4	V
Battery Thermal Protection NTC						
UTP	Under temperature protection		70%	75%	80%	V_{SVIN}
	Under temperature protection hysteresis	Falling edge		5%		
OTP	Over temperature protection		28%	30%	32%	
	Over temperature protection hysteresis	Rising edge		2%		
Thermal Regulation And Thermal shutdown						
T_{REG}	Thermal regulation threshold			120		ºC
T_{REGHYS}	Thermal regulation hysteresis falling edge			20		ºC
	Thermal regulation fold back ratio			0.25		I_{CC}
T_{SD}	Thermal shutdown temperature	Rising Threshold		160		ºC
T_{SDHYS}	Thermal shutdown temperature hysteresis			30		ºC

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

General Function Description

SY6982C is a 3.0-5.5V_{IN}, 2A two-cell synchronous boost Li-Ion battery charger integrates 1MHz switching frequency and full protection functions. The charge current up to 2A can be programmed by using the external resistor for different portable applications and indicates the charger current information simultaneous. It also has a programmable charge timeout and adaptive input current limit for safety battery charge operation. SY6982C can disconnect output when there is output short circuit or shutdown happens. It consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

Charging Status Indication Description

1. Charge-In-Process – Pull and keep STAT pin to Low;
2. Charge Done – Pull and keep STAT pin to High;
3. Fault Mode – Output high and low voltage alternatively with 1.3Hz frequency. Connect a LED from SVIN to STAT pin, LED ON means Charge-in-Process, LED OFF means Charge Done, LED Flashing with 1.3HZ means Fault Mode.

Switching Mode Boost Charger Basic Operation Description

Switching Mode Control Strategy

SY6982C is a switching mode Boost charger for the applications with USB power input. SY6982C utilizes quasi-fixed frequency constant OFF time control to simplify the internal close-loop compensation design. Slope compensation is not necessary for the stable operation. The quasi-fixed frequency settled at 1MHz is easy for the size minimization of peripheral circuit design. During the light load operation, when the output voltage of the internal error amplifier VC is lower than the minimum threshold 0.3V, the OFF time is going to be stretched to achieve frequency fold back.

Operation Principle

SY6982C can normally work with or without Li-Ion battery both.

Battery Present

Before SY6982C start-up, C_{BD} is charged by the battery thru the body diode of blocking FET, and V_{BD} equals to V_{BAT}.

If the plug in input voltage V_{IN} is higher than V_{BD}=V_{BAT}, C_{BD} is charged by V_{IN} further thru the body diode of sync-FET. Under this condition, the Boost charger operates in light load mode and regulates the V_{BD} at 6V and the blocking FET works in linear charge mode. If the V_{BAT} is lower than the internal short circuit threshold V_{SHORT}, the linear charge current is 1/20 I_{CC}. When V_{BAT} is higher than V_{SHORT} but lower than the threshold of trickle charge, the linear charge current is 1/10 of I_{CC}. Note that, charging current would not be increased to I_{CC} when the block FET operates in linear mode. With the increasing of V_{BAT}, when V_{BAT} is higher than both V_{IN} and V_{TRK} the blocking FET is fully turned on and the switching mode boost charger takes over the battery charging. The current in the blocking FET is mirrored to be as the charging current I_{CHG}. If V_{IN} is lower than V_{BD}=V_{BAT} at the plug in time, the switching mode boost charger starts work directly.

During the charging mode, constant (trickle) charging current loop is active first. When V_{BAT} equals to constant voltage threshold V_{CV}, constant voltage loop takes over and pull down the charging current. When I_{CHG} is lower than the termination current threshold I_{TERM}, the main FET of boost charger is turned off firstly. Sync-FET and blocking FETs are turned off together when the current is down to zero. Then, SY6982C is waiting for recharge mode.

Battery Absent

If there's no battery connection detected thru NTC pin, SY6982C operates as a normal switching mode boost converter. When V_{SVIN} is higher than UVLO threshold, the blocking FET is softly turned on. After the blocking FET fully turn-on, switching mode boost converter starts work. The internal current loop and voltage loop are active both.

Basic Protection Principle

SY6982C has fully battery charging protection. When the input over voltage protection, the output over voltage protection, the thermal protection or the timeout protection happens, the main FET of the boost charger is turned off immediately. The sync-FET and the blocking FET are turned off later when the current is down to zero. When the V_{BAT} is lower than V_{SHORT}, the short circuit protection happens. The main FET is turned off firstly. The block FET enters linear mode with 100mA charging current. When V_{BAT} recovers back to be higher than V_{SHORT}, the boost charger restarts to work at light load and regulates V_{BD} at 6V. The linear charge current is increased from 100mA to be trickle current.

Basic Adaptive Input Current Limit Principle

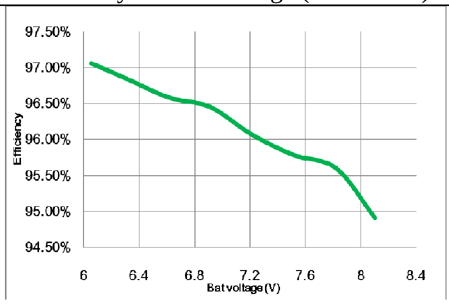
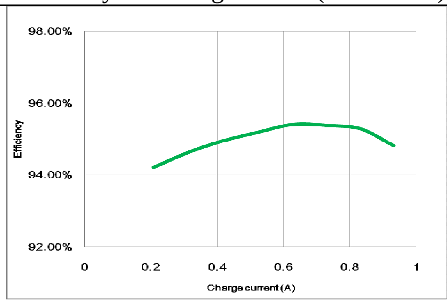
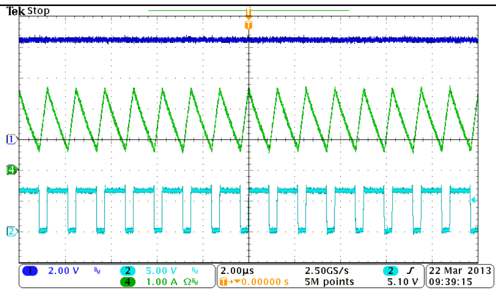
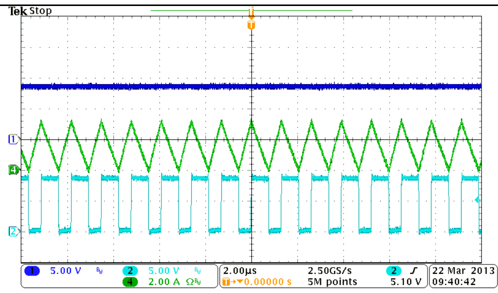
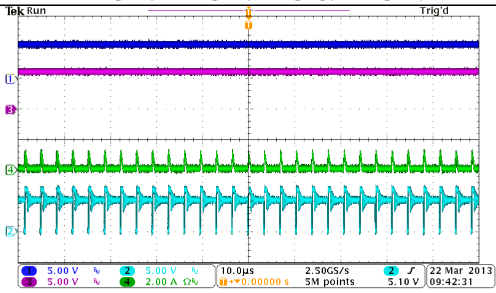
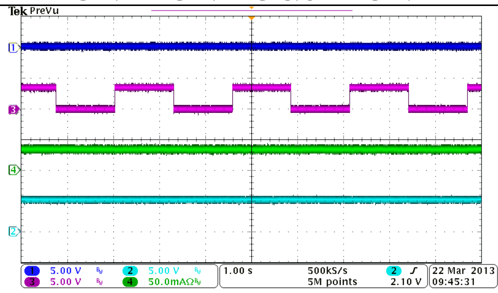
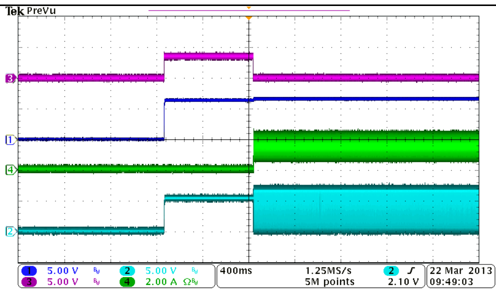
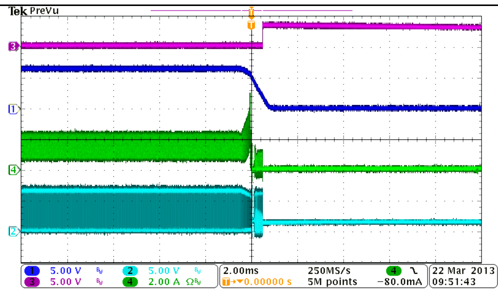
SY6982C has adaptive input current limit function. Before the IC starts charging work, the input voltage is detected and saved as reference V_{INREF}. Once IC starts to charge, the output charging current I_{CHG} is ramped up softly and the V_{IN} drop is monitored simultaneously. When the input voltage drop is larger than V_{DISS} the output charging current reference I_{CHGREF} starts to be discharged slowly and when the voltage drop is larger than V_{DISF} the I_{CHGREF} starts to be fast discharged. With the discharging of I_{CHGREF}, the charging current is deceased and the V_{IN} would recover back. Once the V_{IN} recovers back into the normal range, the I_{CHGREF} is kept on the current value. The I_{CHGREF} would be decreased along with the increasing of output voltage to keep the input power at the maximum value. The internal digital machine state is built up to achieve this function.

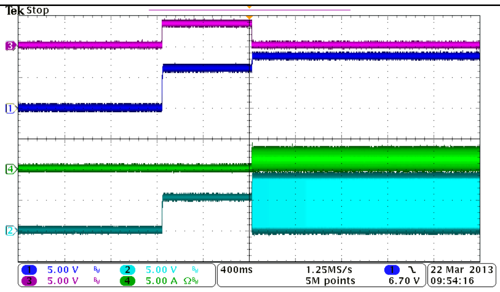
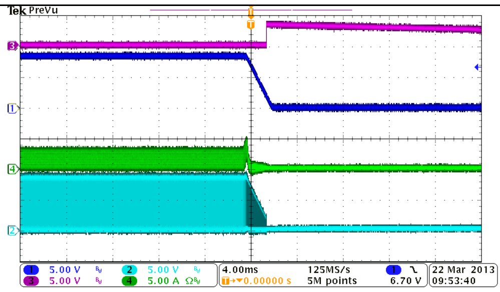
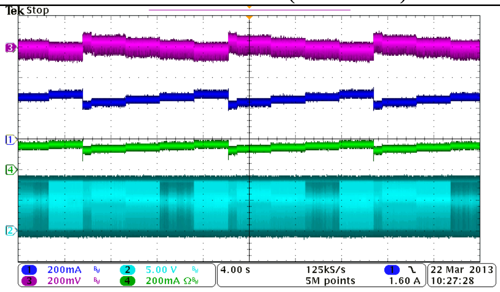
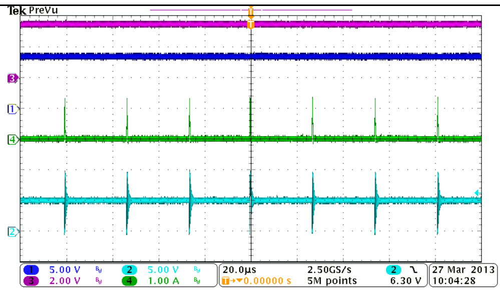
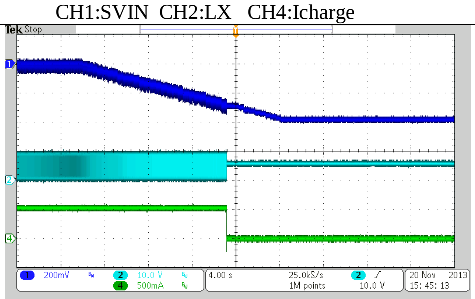
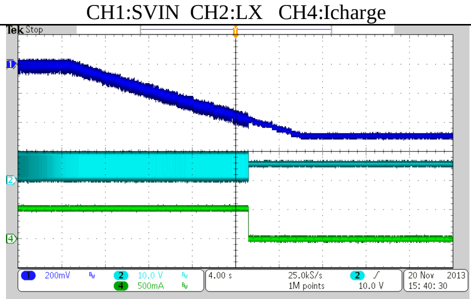
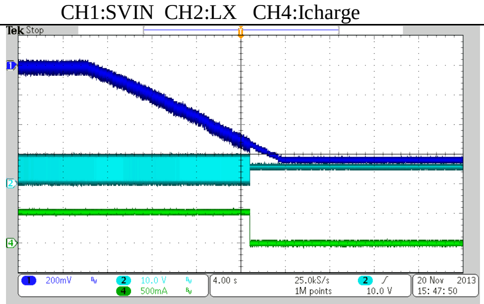
Constant Voltage Threshold Program Principle

SY6982C can program the constant voltage threshold thru the CV pin. When V_{CV} is higher than 2V, the constant voltage threshold is 8.7V; when V_{CV} is lower than 1V, the constant voltage threshold is 8.4V.

Typical Performance Characteristics

T_A=25°C, V_{IN}=5V, R_{RCH}=10kΩ, unless otherwise specified.

Efficiency VS Bat voltage (CC mode)	Efficiency VS Charge current(CV mode)
	
Steady waveforms (CC Mode) CH1:BAT CH2:LX CH4:IL	Steady waveforms (CV Mode) CH1:BAT CH2:LX CH4:IL
	
Steady waveforms (TC Mode) CH1:BAT CH2:LX CH3: BD CH4:IL	Steady waveforms (Short Mode) CH1:BAT CH2:LX CH3: STAT CH4:IL
	
Power on (CC Mode) CH1:BAT CH2:LX CH3: STAT CH4:IL	Power off (CC Mode) CH1:BAT CH2:LX CH3: STAT CH4:IL
	

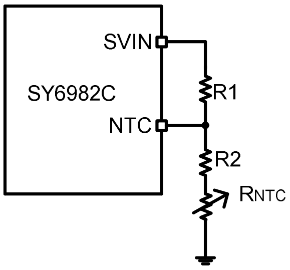
Power on (CV Mode) CH1:BAT CH2:LX CH3: STAT CH4:IL	Power off (CV Mode) CH1:BAT CH2:LX CH3: STAT CH4:IL
	
Adaptive input current limit CH1:Iin CH2:LX CH3: SVIN(Offset=4.8V) CH4:Io	Boost Mode (Null load) CH1:BAT CH2:LX CH3: STAT CH4:IL
	
Different Input Current Limit Threshold (Float ILIM) CH1:SVIN CH2:LX CH4:Icharge	Different Input Current Limit Threshold (Pull low ILIM) CH1:SVIN CH2:LX CH4:Icharge
	
Different Input Current Limit Threshold (Pull high ILIM) CH1:SVIN CH2:LX CH4:Icharge	
	

Applications Information

Because of the high integration of SY6982C, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L, NTC resistors R1,R2 and timer capacitor C_{TIM} need to be selected for the targeted applications specifications.

NTC resistor:

SY6982C monitors battery temperature by measuring the input voltage and NTC voltage. The controller triggers the UTP or OTP when the rate K ($K=V_{NTC}/V_{SVIN}$) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.
Choose R1 and R2 to program the proper UTP and OTP points.



The calculation steps are:

1. Define K_{UT}, K_{UT} =70~80%
2. Define K_{OT}, K_{OT} =28~32%
3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold and R_{OT} at OTP threshold.
4. Calculate R2,

$$R2 = \frac{K_{OT}(1-K_{UT})R_{UT} - K_{UT}(1-K_{OT})R_{OT}}{K_{UT} - K_{OT}}$$

5. Calculate R1

$$R1 = (1/K_{OT} - 1)(R2 + R_{OT})$$

If choose the typical values K_{UT} =75% and K_{OT}=30%, then

$$R2 = 0.17R_{UT} - 1.17R_{OT}$$
$$R1 = 2.3(R2 + R_{OT})$$

Timer capacitor C_{TIM}

The charger also provides a programmable charge timer. The charge time is programmed by the capacitor connected between the TIM pin and GND. The capacitance is given by the formula:

$C_{TIM}=2*10^{-11}T_{CC}$ Unit:F

T_{CC} is the target constant charge time，unit: s.

Input capacitor C_{IN}:

The ripple current through input capacitor is greater than

$$I_{CIN\_RMS} = \frac{V_{IN} * (V_{OUT} - V_{IN})}{2\sqrt{3} * L * F_{SW} * V_{OUT}}$$

X5R or X7R ceramic capacitors with greater than 4.7uF capacitance are recommended to handle this ripple current.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. This ripple voltage is related to the capacitance and its equivalent series resistance (ESR). For the best performance, it is recommended to use X5R or better grade low ESR ceramic capacitor. The voltage rating of the output capacitor should be higher than the maximum output voltage. The minimum required capacitance can be calculated as:

$$C_{OUT} = \frac{I_{CC} * (V_{OUT} - V_{IN})}{F_{SW} \times V_{OUT} \times V_{RIPPLE}}$$

V_{RIPPLE} is the peak to peak output ripple, I_{CC} is the setting charge current.
For SY6982C, output capacitor is paralleled by C_{BD} and C_{BAT}, for smaller output ripple noise, each capacitor with greater than 10uF capacitance is recommended.

Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{I_{CC} \times F_{SW} \times 40\%}$$

Where F_{SW} is the switching frequency and I_{CC} is the setting charge current.
The SY6982C is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

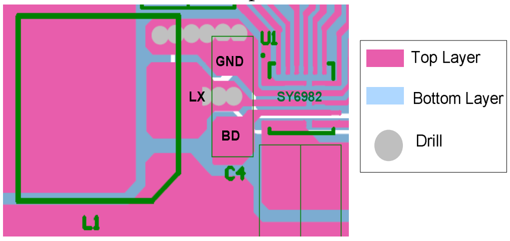
$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{CC} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mohm to achieve a good overall efficiency.

Layout Design:

The layout design of SY6982C regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{SVIN}, L, C_{BD}.

1) The loop of main MOSFET, rectifier diode, and C_{BD} must be as short as possible



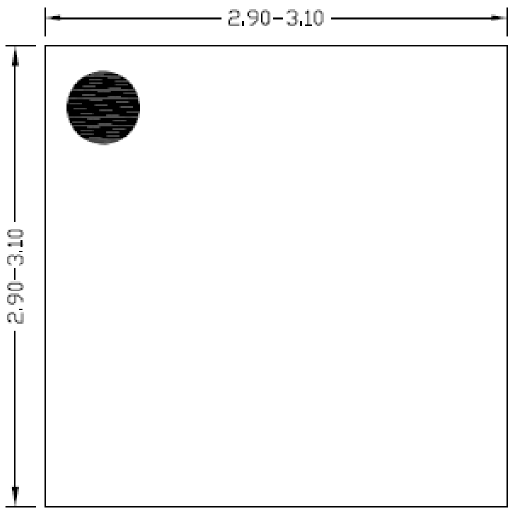
2) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance.

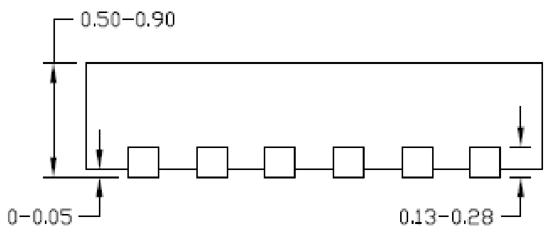
3) C_{SVIN} must be close to pin SVIN and GND.

4) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

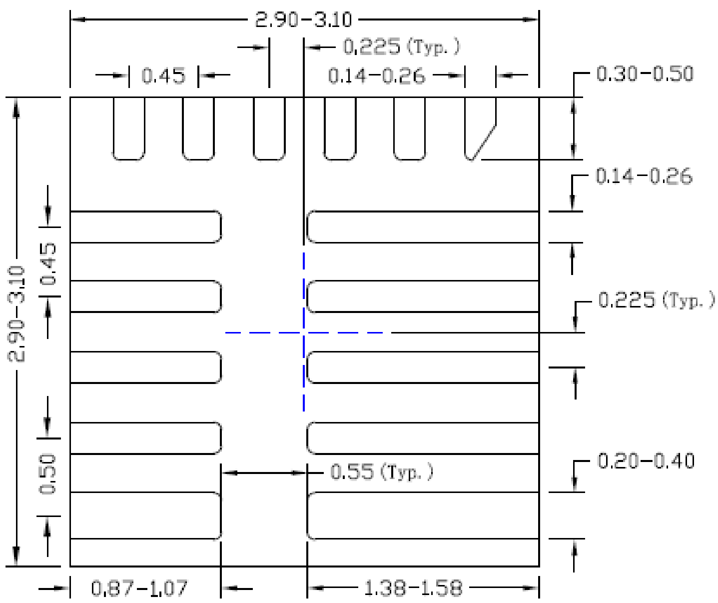
5) The small signal component R_{ICHG} must be placed close to IC and must not be adjacent to the LX net on the PCB layout to avoid the noise problem

QFN3x3-16 FC Package Outline Drawing





Top View **Side View**



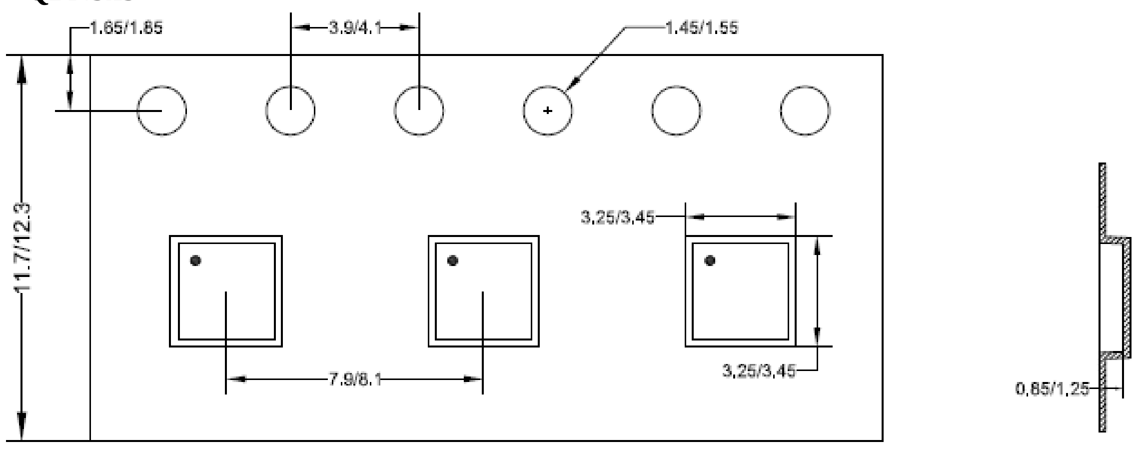
Bottom View

Notes: **All dimension in MM and exclude mold flash & metal burr**

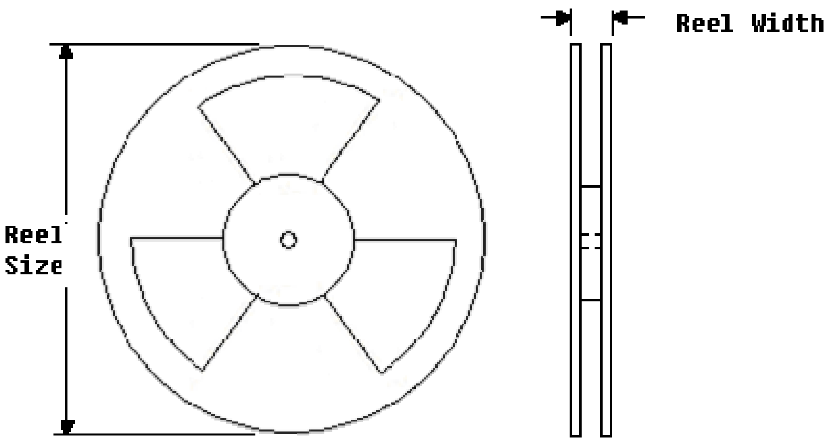
Taping & Reel Specification

1. Taping orientation

QFN3x3



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3x3	12	8	13"	12.4	400	400	5000

3. Others: NA