

Specification for Approval

PRODUCT NAME: QG-2896TDEAF02
REV: A03

CUSTOMER
APPROVED BY
DATE:

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2008. 05. 29	
X02	■ Add the IC specifications ■ Add the lifetime specifications ■ Add the panel electrical specifications ■ Add the application circuit	2008. 07. 03	Page 6~8 & 11~14
X03	■ Modify polarizer	2008. 09. 18	Page 4, 5, 8 & 16
X04	■ Modify D.C electrical characteristics ■ Modify description of VCC pin	2009. 02. 04	Page 7 & 10
X05	■ Modify definition of panel thickness ■ Add the packing specification	2009. 04. 10	Page 5 & 17
A01	■ Transfer from X version ■ Modify polarizer ■ Add the information of module weight	2009. 11. 13	Page 4, 5, 6, 8 & 16
A02	■ Modify seal color (white→black)	2009. 12. 31	Page 16
A03	■ Remove single tape	2013. 07. 25	Page 16

CONTENTS

ITEM	PAGE
<u>1. SCOPE</u>	4
<u>2. WARRANTY</u>	4
<u>3. FEATURES</u>	4
<u>4. MECHANICAL DATA</u>	5
<u>5. MAXIMUM RATINGS</u>	6
<u>6. ELECTRICAL CHARACTERISTICS</u>	7
6.1 D.C ELECTRICAL CHARACTERISTICS	
6.2 ELECTRO-OPTICAL CHARACTERISTICS	
<u>7. INTERFACE</u>	9
7.1 FUNCTION BLOCK DIAGRAM	
7.2 PANEL LAYOUT DIAGRAM	
7.3 PIN ASSIGNMENTS	
7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP	
7.5 INTERFACE TIMING CHART	
<u>8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT</u>	13
8.1 POWER ON / OFF SEQUENCE	
8.2 APPLICATION CIRCUIT	
8.3 COMMAND TABLE	
<u>9. RELIABILITY TEST CONDITIONS</u>	15
<u>10. EXTERNAL DIMENSION</u>	16
<u>11. PACKING SPECIFICATION</u>	17
<u>12. APPENDIXES</u>	18

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by Allvision. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

Allvision warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). Allvision is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, Allvision is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : 262K color and 65K colors
- Panel matrix : 128*96
- Driver IC : SSD1351UR1
- Excellent quick response time.
- Extremely thin thickness for best mechanism design : 1.21mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- 8 bits 6800-series parallel interface, 8 bits 8080-series parallel interface, Serial Peripheral Interface.
- Wide range of operating temperature : -40 to 70 °C
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x 96 (H)	dot
2	Dot Size	0.0435 (W) x 0.1855 (H)	mm ²
3	Dot Pitch	0.0685 (W) x 0.2055 (H)	mm ²
4	Aperture Rate	57	%
5	Active Area	26.279 (W) x 19.708 (H)	mm ²
6	Panel Size	33 (W) x 25.8 (H)	mm ²
7*	Panel Thickness	1.02 ± 0.1	mm
8	Module Size	33 (W) x 46.8 (H) x 1.21 (D)	mm ³
9	Diagonal A/A size	1.29	inch
10	Module Weight	2.3 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{CI})	-0.3	4	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Supply Voltage (V_{CC})	8	21	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Operating Temp.	-40	70	$^\circ\text{C}$		
Storage Temp	-40	85	$^\circ\text{C}$		
Humidity	-	85	%		
Life Time	11,000	-	Hrs	90 cd/m^2 , 50% checkerboard	Note (1)
Life Time	12,000	-	Hrs	80 cd/m^2 , 50% checkerboard	Note (2)

Note:

(A) Under $V_{CC} = 15\text{V}$, $T_a = 25^\circ\text{C}$, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 90 cd/m^2 :

- Master contrast setting : 0x07
- Frame rate : 105Hz
- Duty setting : 1/96

(2) Setting of 80 cd/m^2 :

- Master contrast setting : 0x06
- Frame rate : 105Hz
- Duty setting : 1/96

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

($V_{SS}=0V$, $V_{CI}=2.4$ to $3.5V$, $T_a=25^{\circ}C$)

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Analog power supply (for OLED panel)		14.5	15	15.5	V
V_{CI}	Digital power supply		2.4	2.8	3.5	V
V_{DDIO}	I/O voltage power supply		1.65	1.8	V_{CI}	V
I_{DD}	$V_{CI} = V_{DDIO} = 3.5V$, $V_{CC} = 16V$, External $V_{DD} = 2.6V$, Display ON, No panel attached, contrast = FF			170	190	μA
I_{DDIO}	$V_{CI} = V_{DDIO} = 3.5V$, $V_{CC} = 16V$, Display ON, No panel attached, contrast = FF	External VDD = 2.6V		0.5	10	μA
		Internal VDD		0.5	10	μA
I_{CI}	$V_{CI} = V_{DDIO} = 3.5V$, $V_{CC} = 16V$, Display ON, No panel attached, contrast = FF	External VDD = 2.6V	-	60	70	μA
		Internal VDD		255	280	μA
I_{CC}	$V_{CI} = V_{DDIO} = 3.5V$, $V_{CC} = 16V$, Display ON, No panel attached, contrast = FF	External VDD = 2.6V	-	1.15	1.26	mA
		Internal VDD		1.15	1.26	mA
V_{IH}	Hi logic input level		0.8* V_{DDIO}	-	V_{DDIO}	V
V_{IL}	Low logic input level		0	-	0.2* V_{DDIO}	V
V_{OH}	Hi logic output level		0.9* V_{DDIO}	-	V_{DDIO}	V
V_{OL}	Low logic output level		0	-	0.1* V_{DDIO}	V
I_{SEG}	Segment Output Current Setting $V_{CC} = 16V$ at $I_{REF} = 12.5\mu A$	Contrast=FF	-	200	-	μA
		Contrast=7F	-	100	-	μA
		Contrast=3F	-	50	-	μA

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		20	22	mA	All pixels on (1)
Standby mode current		3	5	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		300	330	mW	All pixels on (1)
Standby mode power consumption		45	75	mW	Standby mode 10% pixels on (2)
Normal Luminance	70	90		cd/m ²	Display Average
Standby Luminance		40		cd/m ²	Display Average
CIE _x (White)	0.24	0.28	0.32		x, y (CIE 1931)
CIE _y (White)	0.28	0.32	0.36		
CIE _x (Red)	0.62	0.66	0.70		
CIE _y (Red)	0.29	0.33	0.37		
CIE _x (Green)	0.26	0.30	0.34		
CIE _y (Green)	0.59	0.63	0.67		
CIE _x (Blue)	0.10	0.14	0.18		
CIE _y (Blue)	0.14	0.18	0.22		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

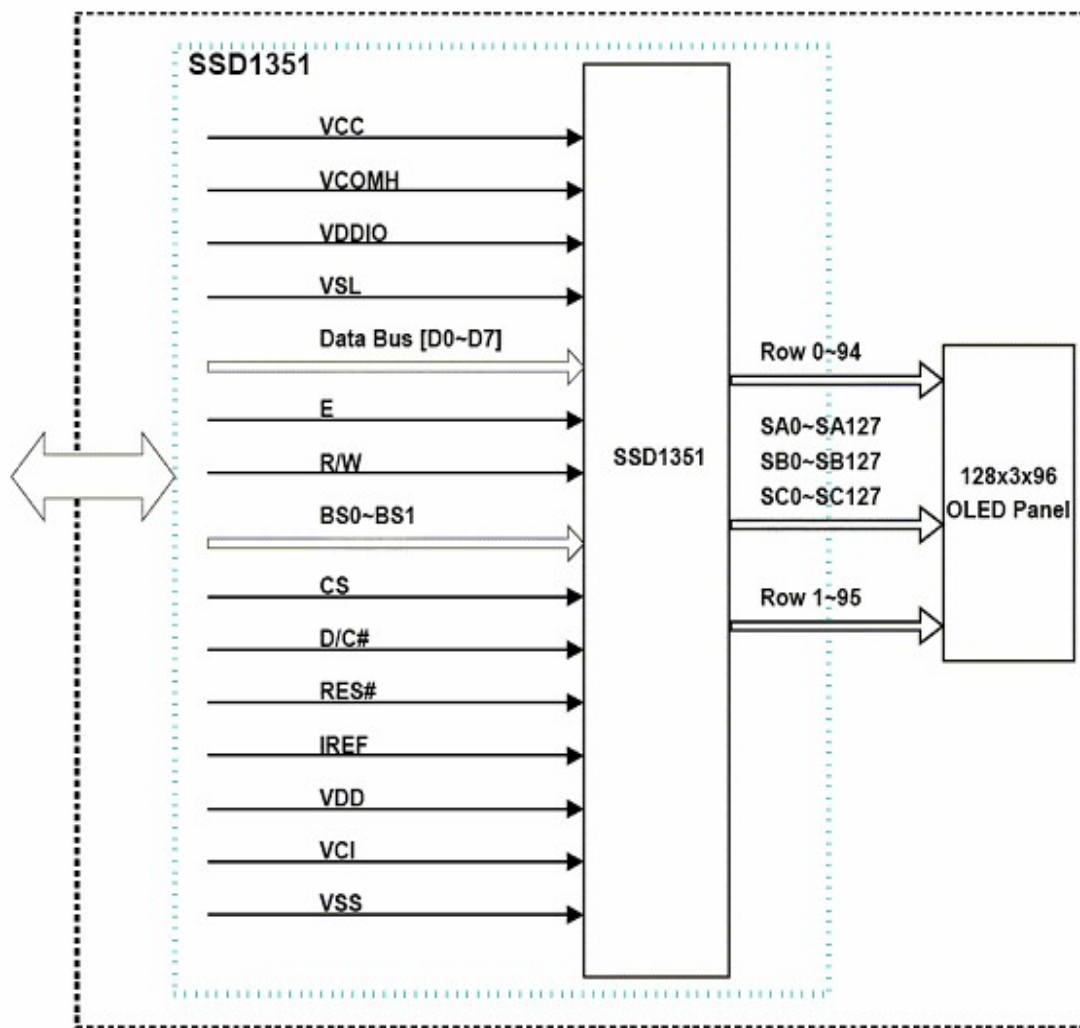
- Driving Voltage : 15V
- Contrast setting : 0x07
- Frame rate : 105Hz
- Duty setting : 1/96

(2) Standby mode condition :

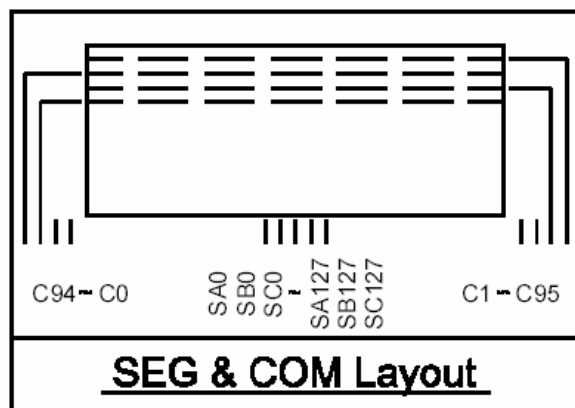
- Driving Voltage : 15V
- Contrast setting : 0x04
- Frame rate : 105Hz
- Duty setting : 1/96

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

PIN NAME	PIN NO	DESCRIPTION
NC	1	No connection.
VCC	2	Power supply for panel driving voltage.
VCOMH	3	COM signal deselected voltage level. A capacitor should be connected between this pin an VSS.
VDDIO	4	Power supply for interface logic level.
VSL	5	This is segment voltage reference pin.
NC	6	No connection.
D7	7	These pins are bi-directional data bus connecting to the MCU data bus.
D6	8	
D5	9	
D4	10	
D3	11	
D2	12	
D1	13	
D0	14	
E	15	8080: data read enable pin; 6800:Read/Write enable pin.
R/W	16	8080: data write enable pin; 6800:Read/Write select pin.
BS0	17	Interface select pin.
BS1	18	Interface select pin.
CS	19	Chip select pin.
D/C#	20	H: Data, L: Command.
RES#	21	Hardware Reset pin (Low active).
IREF	22	A resistor should be connected between this pin and VSS.
NC	23	No connection.
NC	24	No connection.
NC	25	No connection.
VDD	26	Power supply pin for core logic operation.
VCI	27	Digital voltage power supply.
VSS	28	Ground.
VCC	29	Power supply for panel driving voltage.
NC	30	No connection.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 128 x 128 x 18bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

262k Color Depth Graphic Display Data RAM Structure

Segment Address	Normal	0			1			2	126	127			
	Remapped	127			126			125	1	0			
Color		A	B	C	A	B	C	A			C	A	B	C	
Common Address	Data Format	A5	B5	C5	A5	B5	C5	A5	C5	A5	B5	C5	
		A4	B4	C4	A4	B4	C4	A4	C4	A4	B4	C4	
		A3	B3	C3	A3	B3	C3	A3	C3	A3	B3	C3	
		A2	B2	C2	A2	B2	C2	A2	C2	A2	B2	C2	
		A1	B1	C1	A1	B1	C1	A1	C1	A1	B1	C1	
		A0	B0	C0	A0	B0	C0	A0	C0	A0	B0	C0	
Normal	Remapped													Common output	
0	127	6	6	6	6	6	6	6	6	6	6	6	COM0
1	126	6	6	6	6	6	6	6	6	6	6	6	COM1
2	125	6	6	6	6	6	6	6	6	6	6	6	COM2
3	124	6	6	6	6	6	6	6	6	6	6	6	COM3
4	123	6	6	6	6	6	6	6	6	6	6	6	COM4
5	122	6	6	6	6	6	6	6	6	6	6	6	COM5
6	121	6	6	no of bits in this cell			6	6	6	6	6	6	COM6
7	120								6	6	6	6	COM7
:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:
123	4	6	6	6	6	6	6	6	6	6	6	6	:
124	3	6	6	6	6	6	6	6	6	6	6	6	COM124
125	2	6	6	6	6	6	6	6	6	6	6	6	COM125
126	1	6	6	6	6	6	6	6	6	6	6	6	COM126
127	0	6	6	6	6	6	6	6	6	6	6	6	COM127

SEGoutput	SA0	SB0	SC0	SA1	SB1	SC1	SA2	SC126	SA127	SB127	SC127
-----------	-----	-----	-----	-----	-----	-----	-----	-------	-------	-------	-------	-------	-------

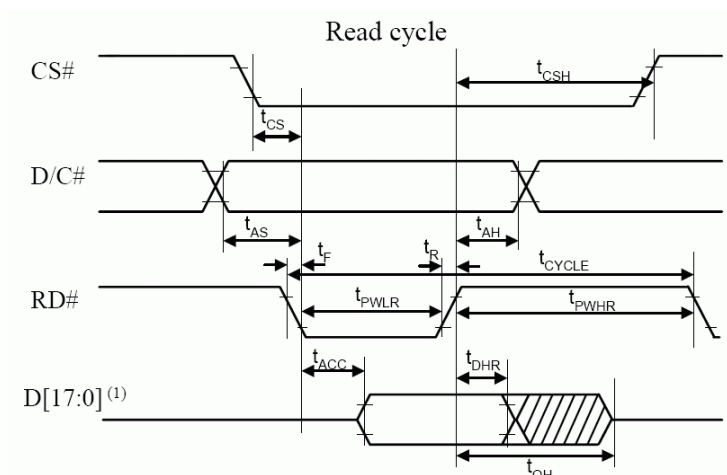
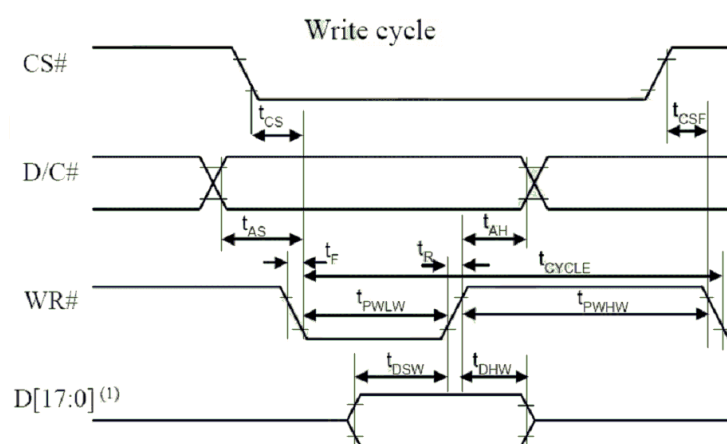
7.5 INTERFACE TIMING CHART

8080-Series MCU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.65V$, $V_{CI} = 2.8V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
$t_{PWL R}$	Read Low Time	150	-	-	ns
$t_{PWL W}$	Write Low Time	60	-	-	ns
$t_{PWH R}$	Read High Time	60	-	-	ns
$t_{PWH W}$	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series MCU parallel interface characteristics



Note

(1) when 8 bit used: D[7:0] instead; when 16 bit used: [15:0] instead; when 18 bit used: D[17:0] instead.

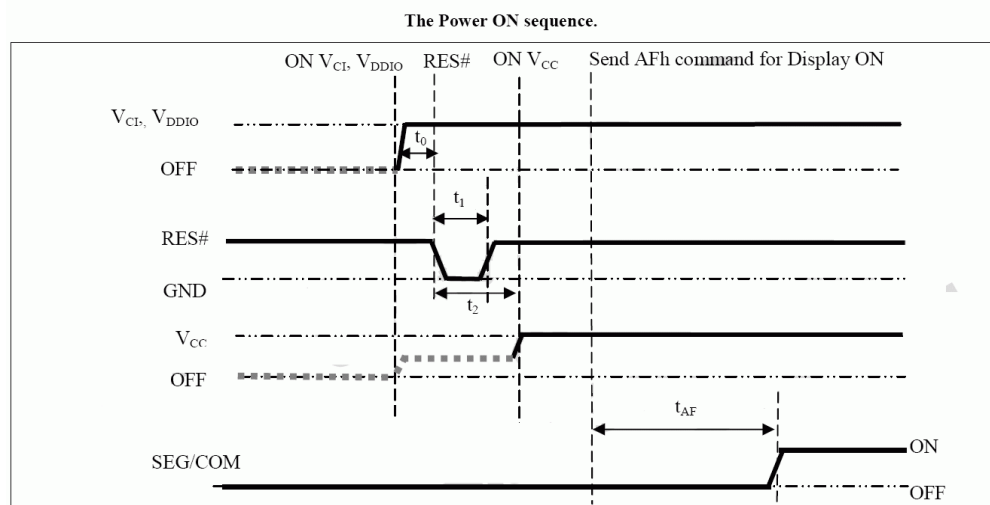
8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

The following figures illustrate the recommended power ON and power OFF sequence of SSD1351 (assume V_{CI} and V_{DDIO} are at the same voltage level and internal V_{DD} is used).

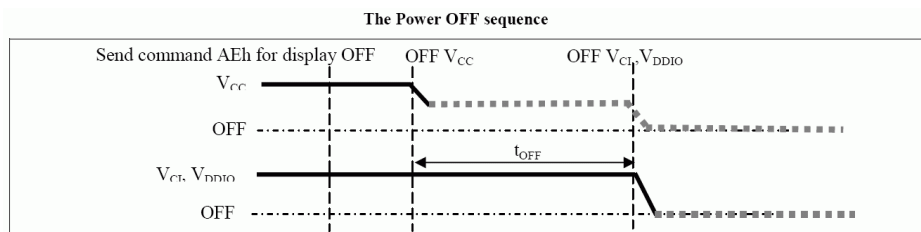
Power ON sequence:

1. Power ON V_{CI} , V_{DDIO} .
2. After V_{CI} , V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 2us (t_1)⁽⁴⁾ and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 2us (t_2). Then Power ON V_{CC} .⁽¹⁾
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).



Power OFF sequence:

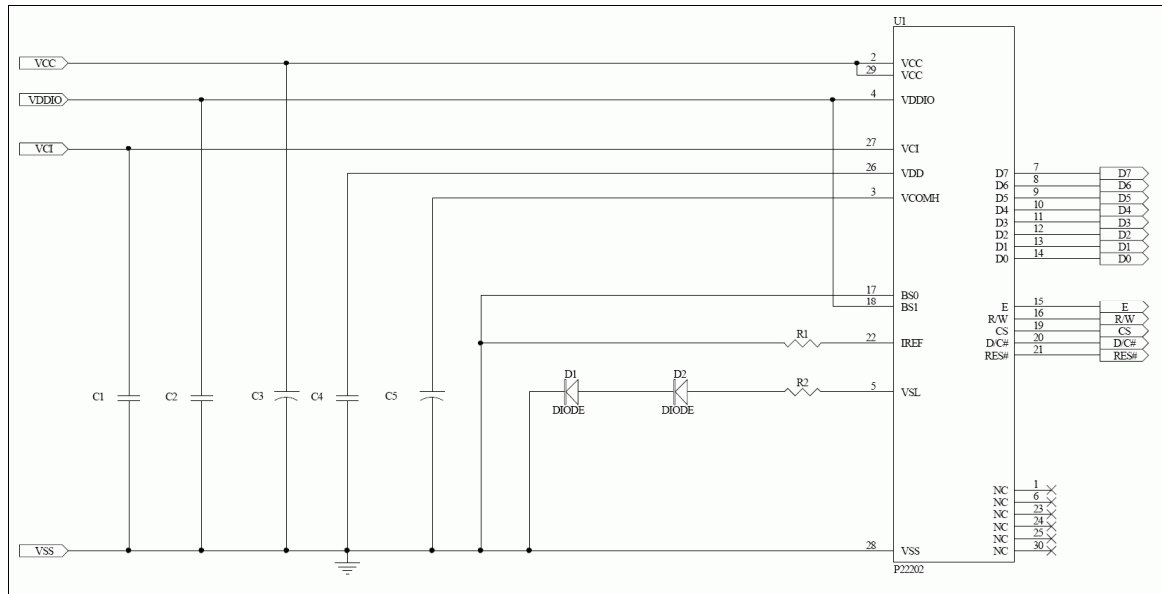
1. Send command AEh for display OFF.
2. Power OFF V_{CC} .^{(1), (2)}
3. Wait for t_{OFF} . Power OFF V_{CI} , V_{DDIO} . (where Minimum $t_{OFF}=80ms$ ⁽³⁾, Typical $t_{OFF}=100ms$)



Note:

- (1) Since an ESD protection circuit is connected between V_{CI} , V_{DDIO} and V_{CC} , V_{CC} becomes lower than V_{CI} whenever V_{CI} , V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
- (2) V_{CC} should be kept float (disable) when it is OFF.
- (3) V_{CI} , V_{DDIO} should not be Power OFF before V_{CC} Power OFF.
- (4) The register values are reset after t_1 .
- (5) Power pins (V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

8.2 APPLICATION CIRCUIT



Recommend components:

C1, C2, C4: 1uF/16V(0805)

C3, C5: 4.7uF/25V or 35V (Tantalum type) or VISHAY (572D475X0025A2T)

R1: 1M ohm 1%(0603)

R2: 50 ohm 1/4W

D1, D2: RB480K(ROHM)

This circuit is for 8080 8bits interface

8.3 COMMAND TABLE

Refer to SSD1351 IC Spec.

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85 °C, 240hrs	5
2	High temp. (Operation)	70 °C, 120hrs	5
3	Low temp. (Operation)	-40 °C, 120hrs	5
4	High temp. / High humidity (Operation)	65 °C, 90%RH, 96hrs	5
5	Thermal shock (Non-operation)	-40 °C ~85 °C (-40 °C /30min; transit /3min; 85 °C /30min; transit /3min) 1cycle: 66min, 20 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle 、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

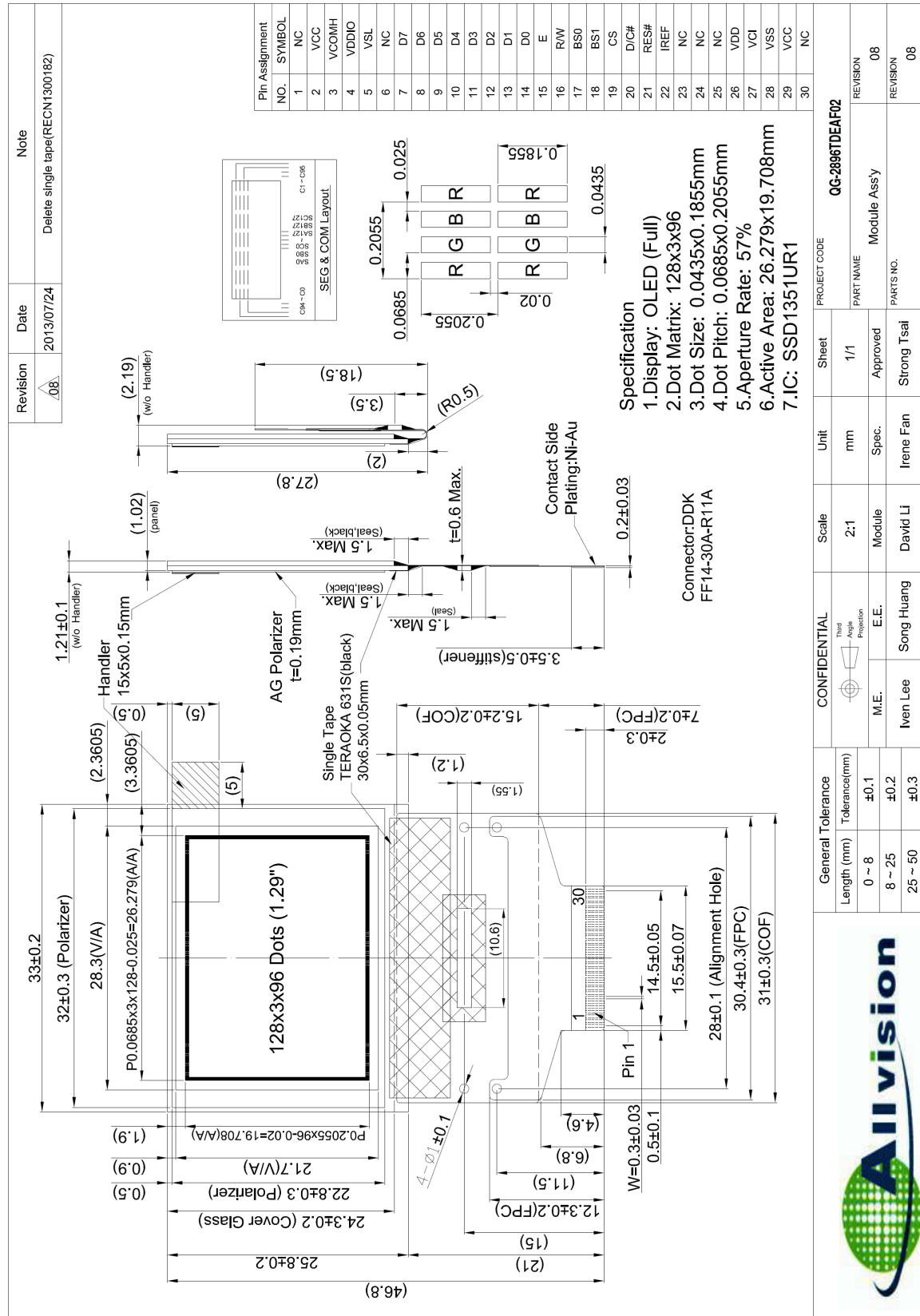
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within $\pm 50\%$ of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION

Revision	Date	Note
02	2009/03/16	Add refer Chinese/English Description

9822202000
Module Assy For P22202 x30 pcs

1 Face up Rotate packing
面朝上, 旋轉放置

3008000209
Tray 330x270x8.7mm T=0.7mm, PS, P22201

3010000002
5G Silica Gel Desiccants
5G 乾燥劑

3010000002
x 1 pcs (empty)

3010000002
x 4 pcs

3003000012
Vacuum Bag ONLY/DPE
真空包裝袋 ONLY/DPE

480x285x90

Vacuum packing : 4 sec
抽真空: 4 秒

3208000125
Tape
膠帶

Tray = 19 pcs

9 Tape
膠帶

3208000125

3003000016
Antistatic Bubble bag 440x(350+450)mm
抗靜電氣泡袋

3001000005
Pizza Box 345x285x88, B corrugated
B 浪

3006000000
Label x2 pcs

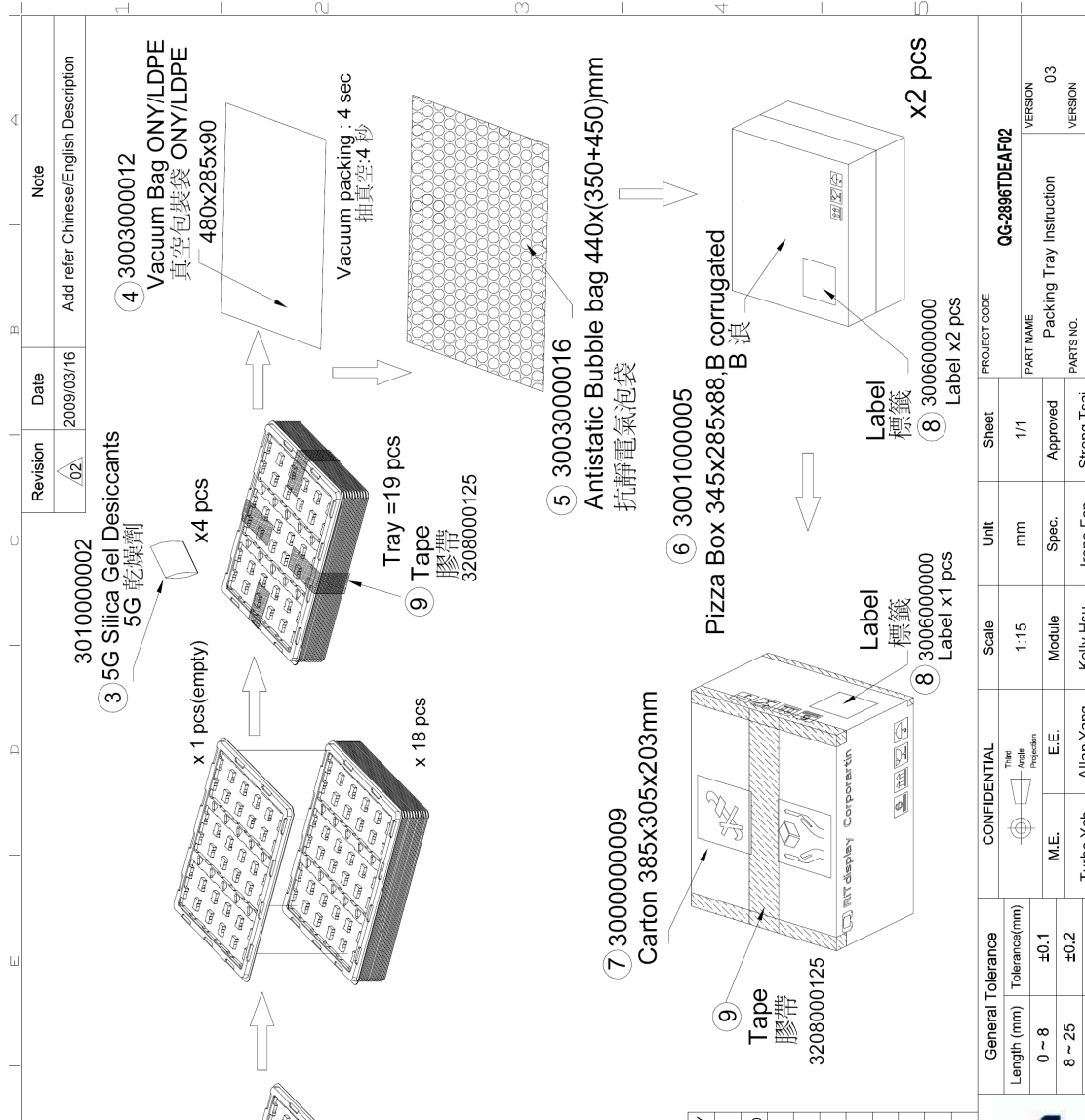
3006000000
Label x2 pcs

3006000000
Label x1 pcs

3006000000
Label x2 pcs


3000000009
Carton 385x305x203mm

3208000125
Tape
膠帶



ITEM	PART No.	DESC	QTY
1	9822202000	Module Assy For P22202	1
2	3008000209	Tray 330x270x8.7 T=0.7mm PS P22201	1080
3	3010000002	5G Silica Gel Desiccants	38
4	3003000012	Vacuum Bag ONLY/DPE 480x285x90	8
5	3003000016	Antistatic Bubble bag 440x(350+450)mm	2
6	3001000005	Pizza Box 345x285x88 B corrugated	2
7	3006000000	Label	1
8	3006000000	Label	3
9	3208000125	Tape, W=48mm, L=9'0cm	

General Tolerance		CONFIDENTIAL		Scale		Unit		Sheet		PROJECT CODE	
Length (mm)	Tolerance (mm)	M.E.	E.E.	1:15	mm	Spec.	Approved	1/1	Q3-2896TDEAF02	PART NAME	VERSION
0 ~ 8	±0.1									Packing Tray Instruction	03
8 ~ 25	±0.2	Turbo Yeh	Allan Yang							PARTS NO.	03
25 ~ 50	±0.3										



12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time T_r is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time T_f is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

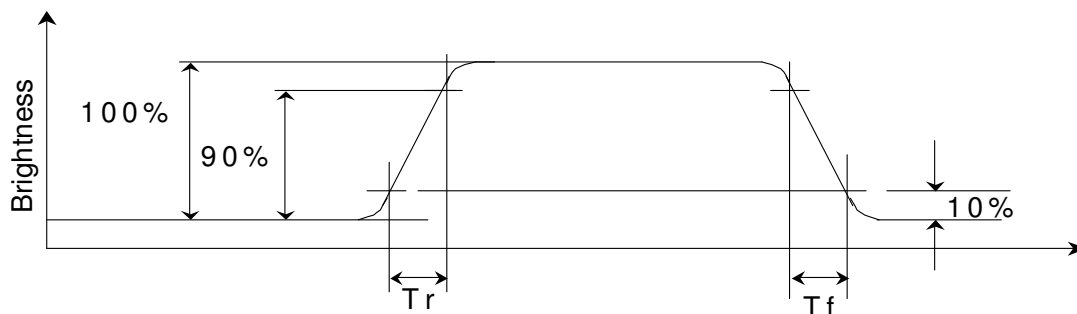


Figure 2: Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

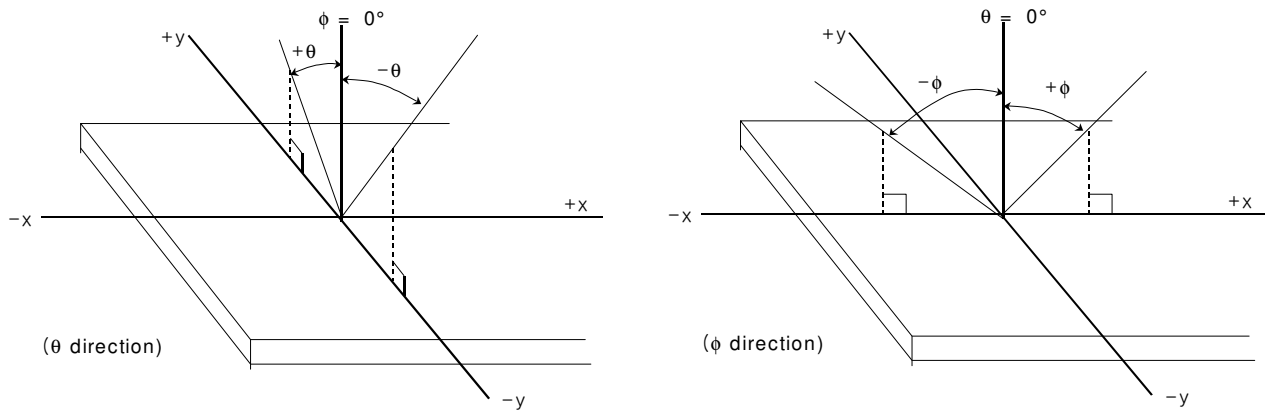
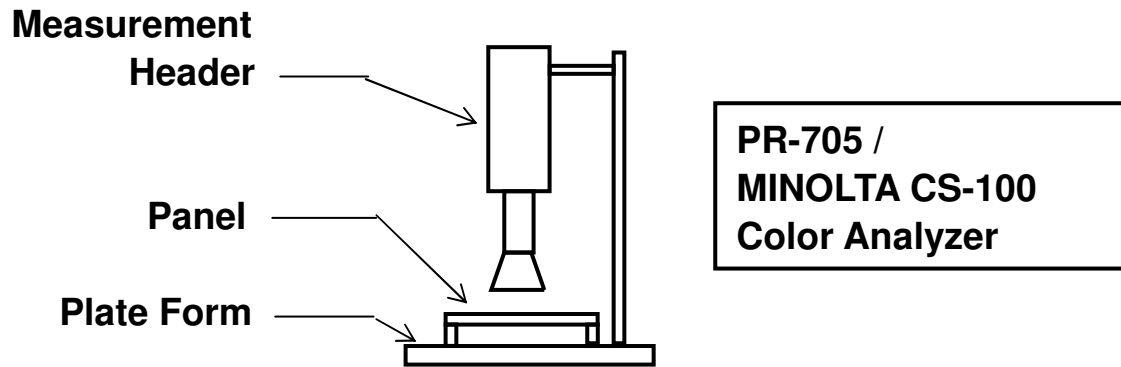


Figure 3: Viewing Angle

APPENDIX 2: MEASUREMENT APPARATUS

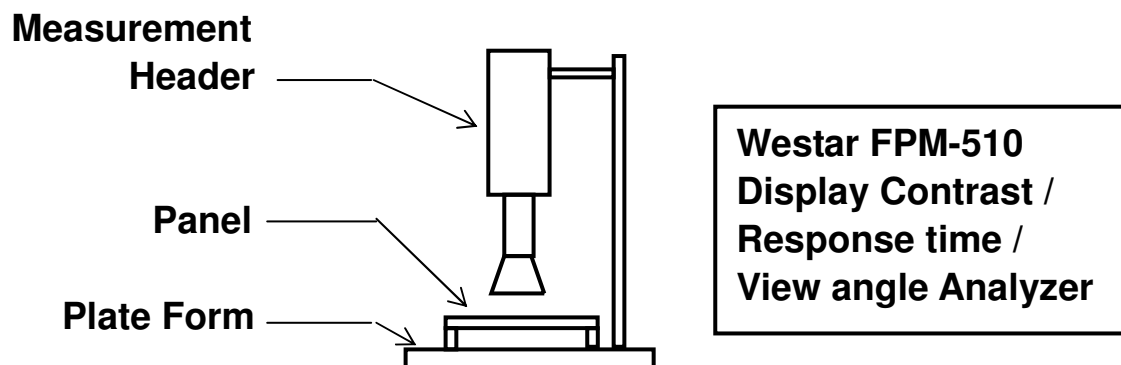
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

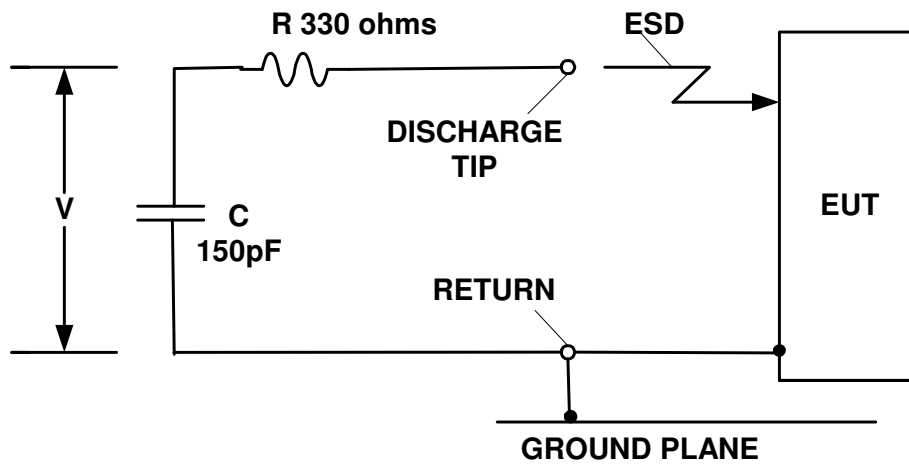


B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.